WM8152

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## Single Channel 16-bit CIS/CCD AFE with 4-bit Wide Output

DESCRIPTION

The WM8152 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 12MSPS.

The device includes a complete analogue signal processing channel containing Reset Level Clamping, Correlated Double Sampling, Programmable Gain and Offset adjust functions. Internal multiplexers allow fast switching of offset and gain for line-by-line colour processing. The output from this channel is time multiplexed into a high-speed 16-bit Analogue to Digital Converter. The digital output data is available in 4-bit wide multiplexed format.

An internal 4-bit DAC is supplied for internal reference level generation. This may be used to reference CIS signals or during Reset Level Clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

Using an analogue supply voltage of 5V, a digital core voltage of 5V, and a digital interface supply of either 5V or 3.3V, the WM8152 typically only consumes 225mW when operating from a single 5V supply.
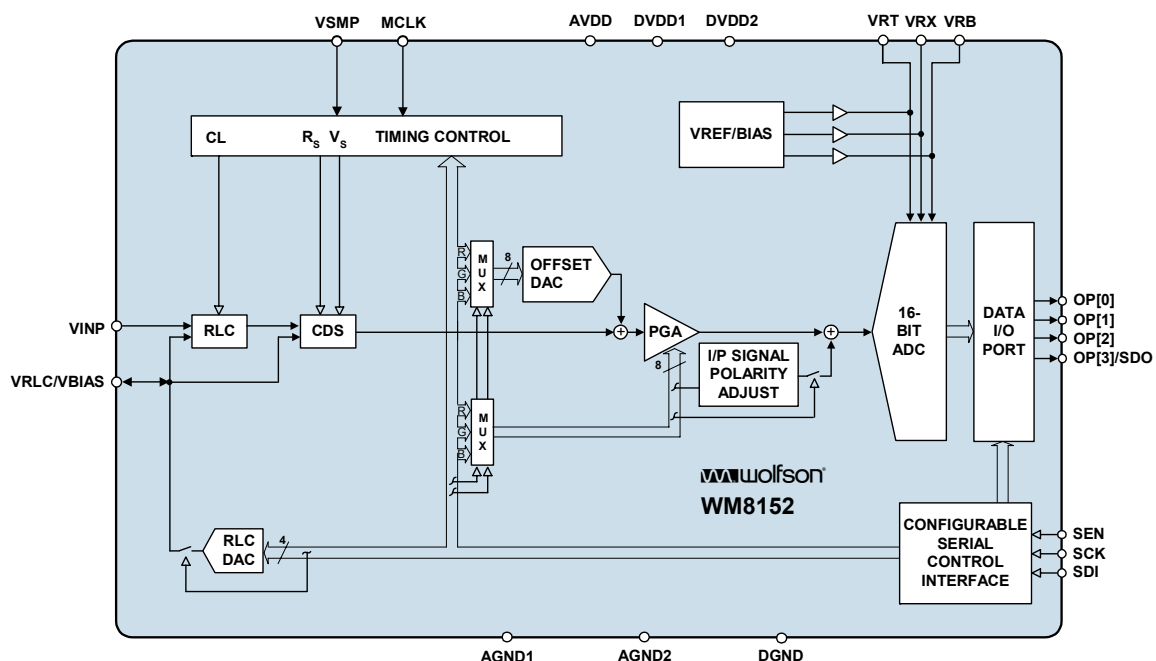
FEATURES

- 16-bit ADC
- 12MSPS conversion rate
- Low power - 225mW typical
- 5V single supply or 5V/3.3V dual supply operation
- Single channel operation
- Correlated double sampling
- Programmable gain (8-bit resolution)
- Programmable offset adjust (8-bit resolution)
- Programmable clamp voltage
- 4-bit wide multiplexed data output format
- Internally generated voltage references
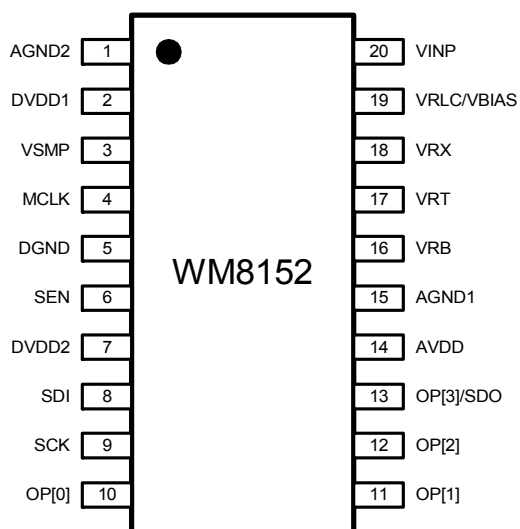- 20-lead SSOP package
- Serial control interface

APPLICATIONS

- Flatbed and sheetfeed scanners
- USB compatible scanners
- Multi-function peripherals
- High-performance CCD sensor interface

BLOCK DIAGRAM

TABLE OF CONTENTS

PIN CONFIGURATION

AGND2	1	20	VINP
DVDD1	2	19	VRLC/VBIAS
VSMP	3	18	VRX
MCLK	4	17	VRT
DGND	5	16	VRB
SEN	6	15	AGND1
DVDD2	7	14	AVDD
SDI	8	13	OP[3]/SDO
SCK	9	12	OP[2]
OP[0]	10	11	OP[1]

WM8152

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8152SCDS/V	0 to 70°C	20-lead SSOP (Pb free)	MSL2	260°C
WM8152SCDS/RV	0 to 70°C	20-lead SSOP (Pb free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION			
1	AGND2	Supply	Analogue ground (0V).			
2	DVDD1	Supply	Digital core (logic and clock generator) supply (5V)			
3	VSMP	Digital input	Video sample synchronisation pulse.			
4	MCLK	Digital input	Master clock. This clock is applied at N times the input pixel rate (N = 2, 3, 6, 8 or any multiple of 2 thereafter depending on input sample mode).			
5	DGND	Supply	Digital ground (0V).			
6	SEN	Digital input	Enables the serial interface when high.			
7	DVDD2	Supply	Digital supply (5V/3.3V), all digital I/O pins.			
8	SDI	Digital input	Serial data input.			
9	SCK	Digital input	Serial clock.			
			Digital multiplexed output data bus. ADC output data (d15:d0) is available in 4-bit multiplexed format as shown below.			
			A	**B**	**C**	**D**
10	OP[0]	Digital output	d12	d8	d4	d0
11	OP[1]	Digital output	d13	d9	d5	d1
12	OP[2]	Digital output	d14	d10	d6	d2
13	OP[3]/SDO	Digital output	d15	d11	d7	d3
			Alternatively, pin OP[3]/SDO may be used to output register read-back data when address bit 4=1 and SEN has been pulsed high. See Serial Interface description in Device Description section for further details.			
14	AVDD	Supply	Analogue supply (5V)			
15	AGND1	Supply	Analogue ground (0V).			
16	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.			
17	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.			
18	VRX	Analogue output	Input return bias voltage. This pin must be connected to AGND via a decoupling capacitor.			
19	VRLC/VBIAS	Analogue I/O	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.			
20	VINP	Analogue input	Video input.			

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD	GND - 0.3V	GND + 7V
Digital core voltage: DVDD1	GND - 0.3V	GND + 7V
Digital IO supply voltage: DVDD2	GND - 0.3V	GND + 7V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 2	GND - 0.3V	GND + 0.3V
Digital inputs, digital outputs and digital I/O pins	GND - 0.3V	DVDD2 + 0.3V
Analogue input (VINP)	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering, 10 seconds)		+260°C
Package body temperature (soldering, 2 minutes)		+183°C

Notes:

1.   GND denotes the voltage of any ground pin.
2.   AGND1, AGND2 and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION		SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range		T_A	0		70	°C
Analogue supply voltage		AVDD	4.75	5.0	5.25	V
Digital core supply voltage		DVDD1	4.75	5.0	5.25	V
Digital I/O supply voltage	5V I/O	DVDD2	4.75	5.0	5.25	V
	3.3V I/O	DVDD2	2.97	3.3	3.63	V

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Performance						
Thermal resistance – junction to case	$R_{\theta JC}$	$T_{ambient}$ = 25°C		32.2		°C/W
Thermal resistance – junction to ambient	$R_{\theta JA}$			81.1		°C/W

Notes:

1.   Figures given are for package mounted on 4-layer FR4 according to JESD51-5 and JESD51-7.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 16-bit ADC, PGA, Offset and CDS functions)						
Full-scale input voltage range (see Note 1)		Max Gain		0.30		Vp-p
		Min Gain		3.22		Vp-p
Input signal limits (see Note 2)	V_{IN}		0		VDD	V
Full-scale transition error		Gain = 0dB; PGA[7:0] = 07(hex)	-50	10	+50	mV
Zero-scale transition error		Gain = 0dB; PGA[7:0] = 07(hex)	-50	10	+50	mV
Differential non-linearity	DNL			1.25		LSB
Integral non-linearity	INL			25		LSB
Total output noise		Min Gain		4.5		LSB rms
		Max Gain		14		LSB rms
References						
Upper reference voltage	VRT			2.70		V
Lower reference voltage	VRB			1.45		V
Input return bias voltage	VRX		1.55	1.65	1.75	V
Diff. reference voltage (VRT-VRB)	V_{RTB}		1.15	1.25	1.35	V
Output resistance VRT, VRB, VRX				1		Ω
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance			20	50	100	Ω
VRLC short-circuit current			1.86	2	4.5	mA
VRLC output resistance				2		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				4		bits
RLCDAC step size, RLCDAC = 0	$V_{RLCSTEP}$	AVDD = 5.0V	0.23	0.25	0.27	V/step
RLCDAC step size, RLCDAC = 1	$V_{RLCSTEP}$		0.14	0.16	0.20	V/step
RLCDAC output voltage at code 0(hex), RLCDACRNG = 0	V_{RLCBOT}	AVDD = 5.0V	0.34	0.39	0.44	V
RLCDAC output voltage at code 0(hex), RLCDACRNG = 1	V_{RLCBOT}		0.20	0.26	0.31	V
RLCDAC output voltage at code F(hex) RLCDACRNG, = 0	V_{RLCTOP}	AVDD = 5.0V	4.0	4.16	4.3	V
RLCDAC output voltage at code F(hex), RLCDACRNG = 1	V_{RLCTOP}		2.56	2.66	2.76	V
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.1	0.5	LSB
Integral non-linearity	INL			0.25	1	LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex)	-247	-260	-273	mV
		Code FF(hex)	+247	+260	+273	mV

Notes:

1. **Full-scale input voltage** denotes the peak input signal amplitude that can be gained to match the ADC input range.

2. **Input signal limits** are the limits within which the full-scale input voltage signal must lie.

Test Conditions

AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Gain Amplifier						
Resolution				8		bits
Gain equation				$0.78 + \dfrac{PGA[7:0] \times 7.57}{255}$		V/V
Max gain	G_{MAX}		6.8	8.35	8.7	V/V
Min gain	G_{MIN}		0.75	0.78	0.82	V/V
Gain error				1	2	%
Internal channel offset	V_{OFF}			10		mV
Analogue to Digital Converter						
Resolution				16		bits
Maximum Speed			12			MSPS
Full-scale input range (2*(VRT-VRB))	V_{FS}			2.5		V
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * DVDD2			V
Low level input voltage	V_{IL}				0.2 * DVDD2	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Supply Currents						
Total supply current – active				45		mA
Total analogue AVDD, supply current – active	I_{AVDD}			41		mA
Total digital core, DVDD1, supply current – active	I_{DVDD1}			3		mA
Digital I/O supply current, DVDD2 – active (see note 3)	I_{DVDD2}			3		mA
Supply current – full power down mode				300	400	µA

Notes:

3.   Digital I/O supply current depends on the capacitive load attached to the pin. The Digital I/O supply current is measured with approximately 50pF attached to the pin.

INPUT VIDEO SAMPLING

Figure 1 Input Video Timing

Note:

1.   See Page 15 (Programmable VSMP Detect Circuit) for video sampling description.

Test Conditions
VDD = 5.0V, DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		41.6			ns
MCLK high period	t_{MCLKH}		18.8			ns
MCLK low period	t_{MCLKL}		18.8			ns
VSMP set-up time	t_{VSMPSU}		6			ns
VSMP hold time	t_{VSMPH}		3			ns
Video level set-up time	t_{VSU}		10			ns
Video level hold time	t_{VH}		3			ns
Reset level set-up time	t_{RSU}		10			ns
Reset level hold time	t_{RH}		3			ns

Notes:

1. t_{VSU} and t_{RSU} denote the set-up time required after the input video signal has settled.
2.   Parameters are measured at 50% of the rising/falling edge.

OUTPUT DATA TIMING
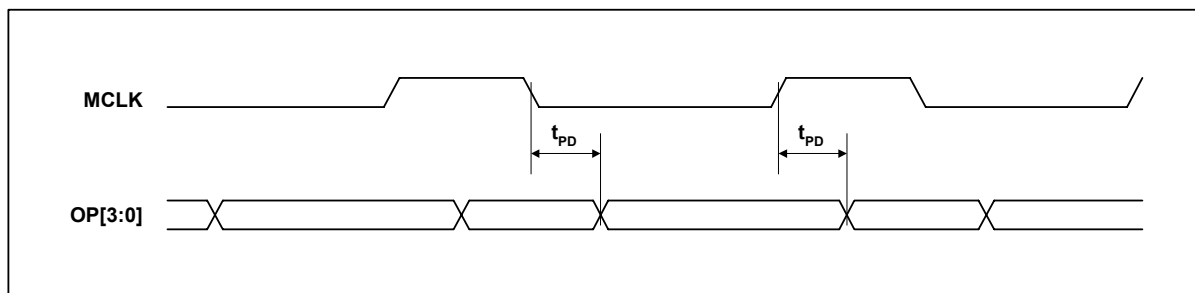
Figure 2 Output Data Timing

Test Conditions
VDD = 5.0V, DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

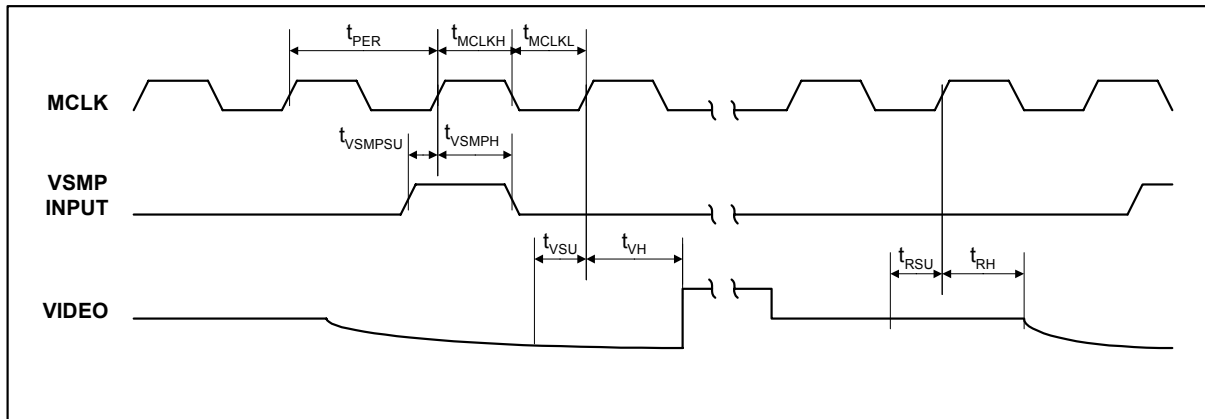| PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}	I_{OH} = 1mA, I_{OL} = 1mA			20	ns

SERIAL INTERFACE
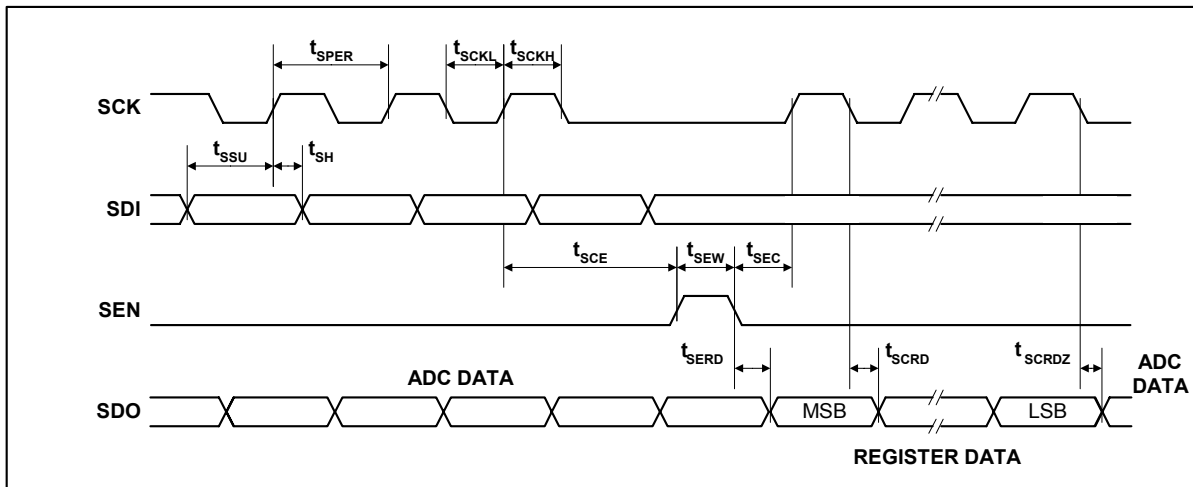
Figure 3 Serial Interface Timing

Test Conditions

VDD = 5.0V, DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		41.6			ns
SCK high	t_{SCKH}		18.8			ns
SCK low	t_{SCKL}		18.8			ns
SDI set-up time	t_{SSU}		6			ns
SDI hold time	t_{SH}		6			ns
SCK to SEN set-up time	t_{SCE}		12			ns
SEN to SCK set-up time	t_{SEC}		12			ns
SEN pulse width	t_{SEW}		25			ns
SEN low to SDO = Register data	t_{SERD}				30	ns
SCK low to SDO = Register data	t_{SCRD}				30	ns
SCK low to SDO = ADC data	t_{SCRDZ}				30	ns

Note:

1.   Parameters are measured at 50% of the rising/falling edge

INTERNAL POWER ON RESET CIRCUIT
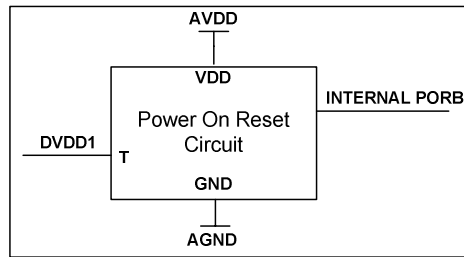
Figure 4 Internal Power On Reset Circuit Schematic

The WM8152 includes an internal Power-On-Reset Circuit, as shown in Figure 4, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD1. It asserts PORB low if AVDD or DVDD1 is below a minimum threshold.

The power supplies can be brought up in any order but is important that either AVDD is brought up and is stable before DVDD comes up or vice versa as shown in Figure 5 and Figure 6.
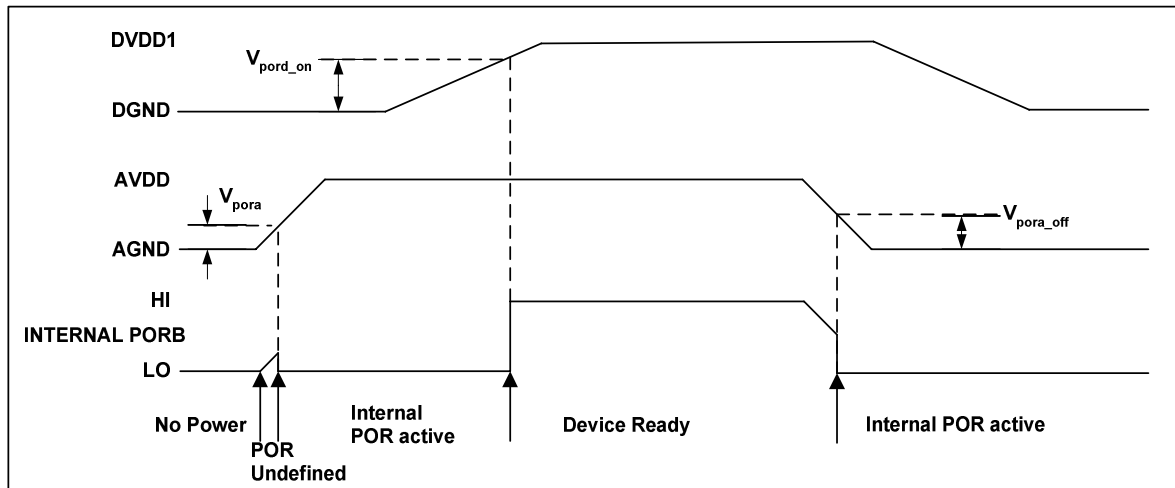
Figure 5 Typical Power up Sequence where AVDD is Powered before DVDD1

Figure 5 shows a typical power-up sequence where AVDD is powered up first. When AVDD rises above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD1 rises to Vpord_on and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.
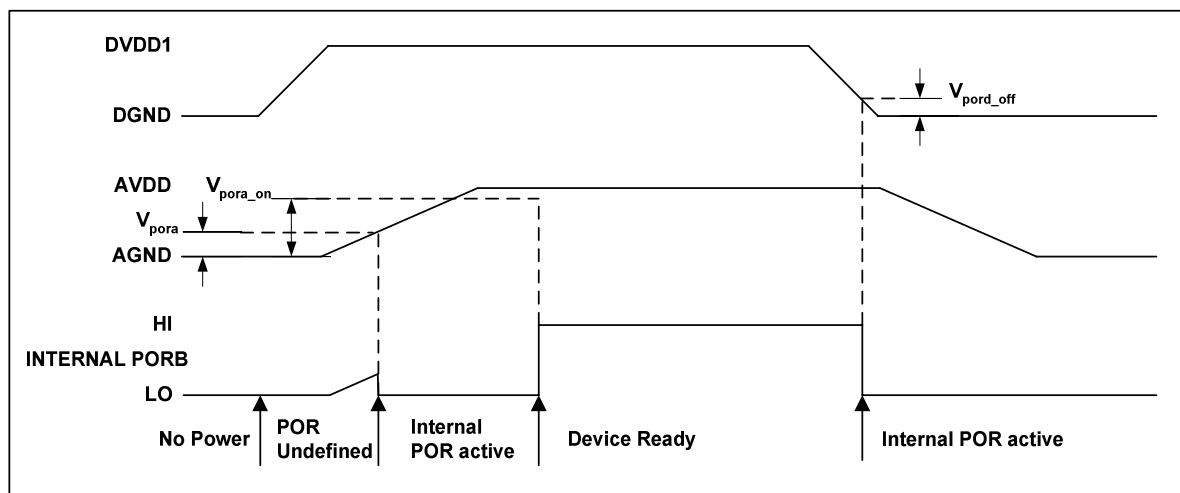
Figure 6 Typical Power up Sequence where DVDD1 is Powered before AVDD

Figure 6 shows a typical power-up sequence where DVDD1 is powered up first. It is assumed that DVDD1 is already up to specified operating voltage. When AVDD goes above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to Vpora_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD1 falls first, PORB is asserted low whenever DVDD1 drops below the minimum threshold Vpord_off.

SYMBOL	TYP	UNIT
V_{pora}	0.6	V
V_{pora_on}	1.2	V
V_{pora_off}	0.6	V
V_{pord_on}	0.7	V
V_{pord_off}	0.6	V

Table 1 Typical POR Operation (typical values, not tested)

Note: It is recommended that every time power is cycled to the WM8199 a software reset is written to the software register to ensure that the contents of the control registers are at their default values before carrying out any other register writes.

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on Page 1.

The WM8152 processes the sampled video signal on VINP with respect to the video reset level or an internally/externally generated reference level through the analogue processing channel.

This processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and an 8-bit Programmable Gain Amplifier (PGA).

The ADC then converts each resulting analogue signal to a 16-bit digital word. The digital output from the ADC is presented on a 4-bit wide bus.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

INPUT SAMPLING

The WM8152 has a single analogue processing channel and ADC which can be used in a flexible manner to process both monochrome and line-by-line colour inputs.

Monochrome: VINP is sampled, processed by the analogue channel, and converted by the ADC. The same offset DAC and PGA register values are always applied.

Colour Line-by-Line: VINP is sampled and processing by the analogue channel before being converted by the ADC. The gains and offset register values applied to the PGA and offset DAC can be switched between the independent Red, Green and Blue digital registers (e.g. Red → Green→ Blue → Red…) at the start of each line in order to facilitate line-by-line colour operation. The INTM[1:0] bits determine which register contents are applied (see Table 2) to the PGA and offset DAC. By using the INTM[1:0] bits to select the desired register values only one register write is required at the start of each new colour line.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8152 VINP pin lies within the valid input range (0V to VDD) the CCD output signal is usually level shifted by coupling through a capacitor, C_{IN}. When active, the RLC circuit clamps the WM8152 side of this capacitor to a suitable voltage during the CCD reset period. The RLCINT register bit controls is used to activate the Reset Level Clamp circuit.

A typical input configuration is shown in Figure 7. The Timing Control Block generates an internal clamp pulse, CL, from MCLK and VSMP (when RLCINT is high). When CL is active the voltage on the WM8152 side of C_{IN}, at VINP, is forced to the VRLC/VBIAS voltage (V_{VRLC}) by closing switch 1. When the CL pulse turns off, switch 1 opens the voltage at VINP initially remains at V_{VRLC} but any subsequent variation in sensor voltage (from reset to video level) will couple through C_{IN} to VINP.

RLC is compatible with both CDS and non-CDS operating modes, as selected by switch 2. Refer to the CDS/non-CDS Processing section.
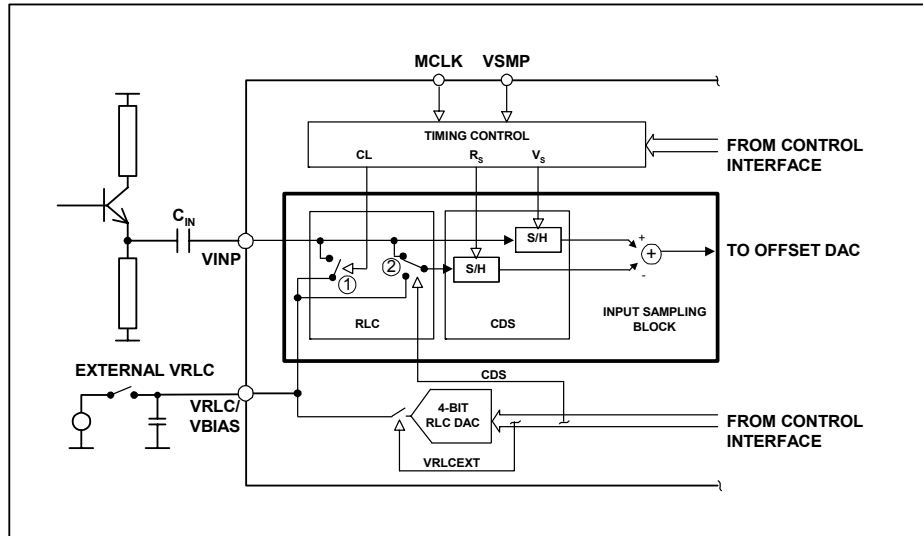
Figure 7 Reset Level Clamping and CDS Circuitry

Reset Level Clamping is controlled by register bit RLCINT. Figure 8 illustrates the effect of the RLCINT bit for a typical CCD waveform, with CL applied during the reset period.

The RLCINT register bit is sampled on the positive edge of MCLK that occurs during each VSMP pulse. The sampled level, high (or low) controls the presence (or absence) of the internal CL pulse on the next reset level. The position of CL can be adjusted by using control bits CDSREF[1:0] (Figure 9).
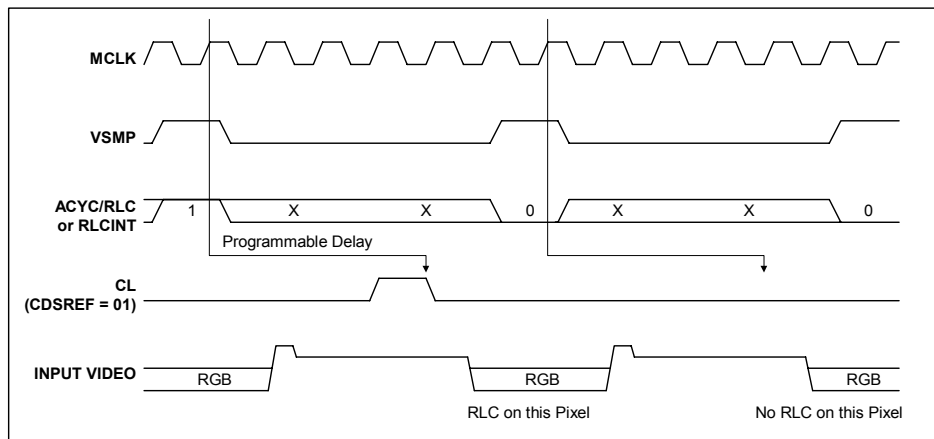
Figure 8 Relationship of RLCINT, MCLK and VSMP to Internal Clamp Pulse, CL

The VRLC/VBIAS pin can be driven internally by a 4-bit DAC (RLCDAC) by writing to control bits RLCV[3:0]. The RLCDAC range and step size may be increased by writing to control bit RLCDACRNG. Alternatively, the VRLC/VBIAS pin can be driven externally by writing to control bit VRLCEXT to disable the RLCDAC and then applying a d.c. voltage to the pin.

CDS/NON-CDS PROCESSING

For CCD type input signals, the signal may be processed using CDS, which will remove pixel-by-pixel common mode noise. For CDS operation, the video level is processed with respect to the video reset level, regardless of whether RLC has been performed. To sample using CDS, control bit CDS must be set to 1 (default), this sets switch 2 into the position shown in (Figure 7) and causes the signal reference to come from the video reset level. The time at which the reset level is sampled, by clock R_s/CL, is adjustable by programming control bits CDSREF[1:0], as shown in Figure 9.
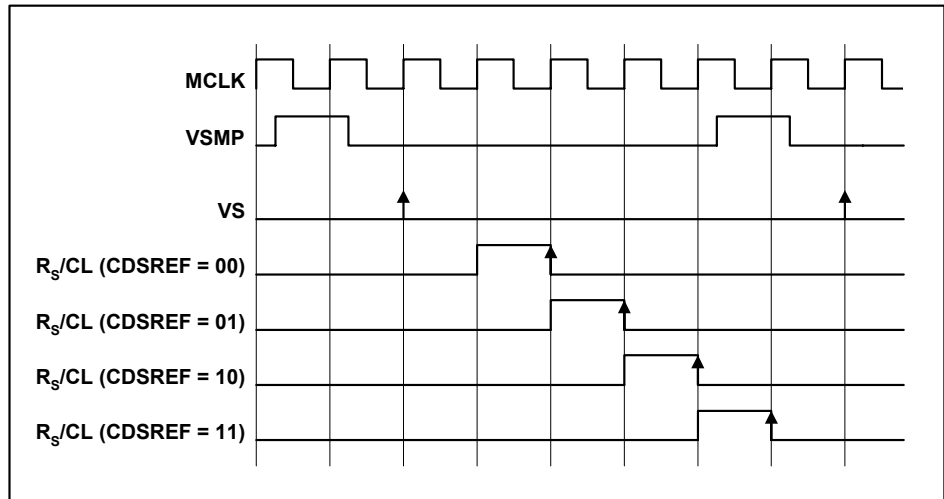
Figure 9 Reset Sample and Clamp Timing

For CIS type sensor signals, non-CDS processing is used. In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS, generated internally or externally as described above. The VRLC/VBIAS pin is sampled by R_s at the same time as V_s samples the video level in this mode; non-CDS processing is achieved by setting switch 2 in the lower position, CDS = 0.

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by an 8-bit PGA. The gain and offset can be set for each of three colours by writing to control bits DACx[7:0] and PGAx[7:0] (where x can be R, G or B).

In colour line-by-line mode the gain and offset coefficients that are applied to the PGA and offset DAC can be multiplexed by control of the INTM[1:0] bits as shown in Table 2.

INTM[1:0]	DESCRIPTION
00	Red offset and gain registers are applied to offset DAC and PGA (DACR[7:0] and PGAR[7:0])
01	Green offset and gain registers applied to offset DAC and PGA (DACG[7:0] and PGAG[7:0])
10	Blue offset and gain registers applied to offset DAC and PGA (DACB[7:0] and PGAB[7:0])
11	Reserved.

Table 2 Offset DAC and PGA Register Control

The gain characteristic of the WM8152 PGA is shown in Figure 10. Figure 11 shows the maximum input voltage (at VINP) that can be gained up to match the ADC full-scale input range (2.5V).
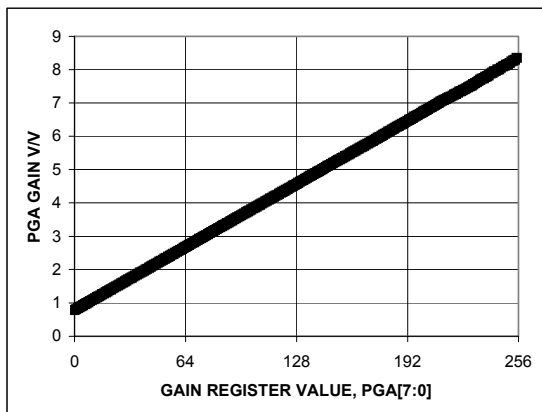
Figure 10 PGA Gain Characteristic
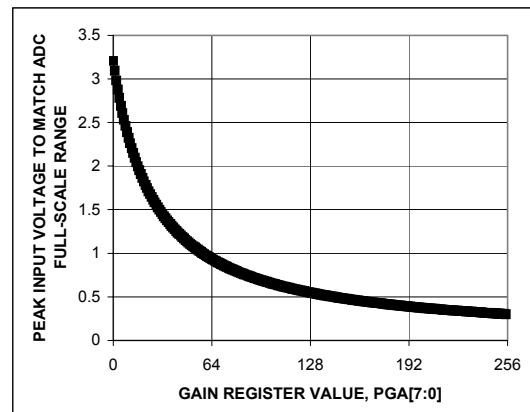
Figure 11 Peak Input Voltage to Match ADC Full-scale

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA should be offset to match the full-scale range of the ADC (V_{FS} = 2.5V). For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. For positive going input signal the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. Bipolar input video is accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01 (zero differential input voltage gives mid-range ADC output).

OVERALL SIGNAL FLOW SUMMARY

Figure 12 represents the processing of the video signal through the WM8152.
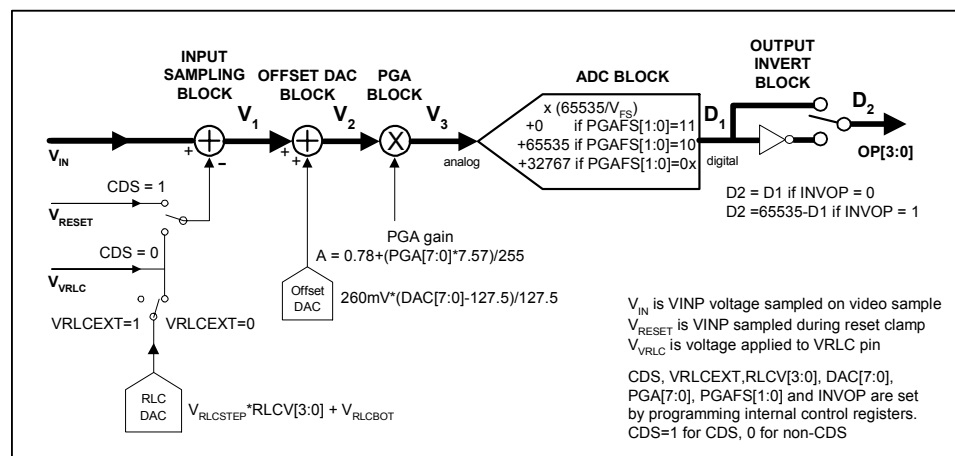
Figure 12 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage **V_1**. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing **V_2**.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage **V_3**.

The **ADC BLOCK** then converts the analogue signal, **V_3**, to a 16-bit unsigned digital output, **D_1**.

The digital output is then inverted, if required, through the **OUTPUT INVERT BLOCK** to produce **D_2**.

CALCULATING OUTPUT FOR ANY GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8152. The values of V_1 V_2 and V_3 are often calculated in reverse order during device setup. The PGA value is written first to set the input Voltage range, the Offset DAC is then adjusted to compensate for any Black/Reset level offsets and finally the RLC DAC value is set to position the reset level correctly during operation.

Note: Refer to WAN0123 for detailed information on device calibration procedures.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video.

$$V_1 \quad = \quad V_{IN} - V_{RESET} \quad\text{...}\quad \text{Eqn. 1}$$

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$V_1 \quad = \quad V_{IN} - V_{VRLC} \quad\text{...}\quad \text{Eqn. 2}$$

If VRLCEXT = 1, V_{VRLC} is an externally applied voltage on pin VRLC/VBIAS.

If VRLCEXT = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} \quad = \quad (V_{RLCSTEP} * RLCV[3:0]) + V_{RLCBOT} \quad\text{.................................}\quad \text{Eqn. 3}$$

$V_{RLCSTEP}$ is the step size of the RLC DAC and V_{RLCBOT} is the minimum output of the RLC DAC.

OFFSET DAC BLOCK: OFFSET (BLACK-LEVEL) ADJUST

The resultant signal V_1 is added to the Offset DAC output.

$$V_2 \quad = \quad V_1 + \{260mV * (DAC[7:0]-127.5)\} / 127.5 \quad\text{......................}\quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain,

$$V_3 \quad = \quad V_2 * [0.78+(PGA[7:0]*7.57)/255] \quad\text{....................................}\quad \text{Eqn. 5}$$

ADC BLOCK: ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

$$D_1[15:0] = INT\{ (V_3 /V_{FS}) * 65535\} + 32767 \quad PGAFS[1:0] = 00 \text{ or } 01 \quad\text{......}\quad \text{Eqn. 6}$$

$$D_1[15:0] = INT\{ (V_3 /V_{FS}) * 65535\} \qquad\qquad PGAFS[1:0] = 11 \quad\text{...............}\quad \text{Eqn. 7}$$

$$D_1[15:0] = INT\{ (V_3 /V_{FS}) * 65535\} + 65535 \quad PGAFS[1:0] = 10 \quad\text{...............}\quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS} = 2.5V

$$\text{if } D_1[15:0] < 0 \qquad D_1[15:0] = 0$$

$$\text{if } D_1[15:0] > 65535 \quad D_1[15:0] = 65535$$

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$D_2[15:0] = D_1[15:0] \qquad\qquad (INVOP = 0) \quad\text{......................}\quad \text{Eqn. 9}$$

$$D_2[15:0] = 65535 - D_1[15:0] \qquad (INVOP = 1) \quad\text{......................}\quad \text{Eqn. 10}$$

OUTPUT DATA FORMAT

The digital data output from the ADC is available to the user in 4-bit wide multiplexed. Latency of valid output data with respect to VSMP is programmable by writing to control bits DEL[1:0]. The latency for each mode is shown in the Operating Mode Timing Diagrams section.

Figure 13 shows the output data formats for Mode 1 and 3 – 6. Figure 14 shows the output data formats for Mode 2. Table 3 summarises the output data obtained for each format.
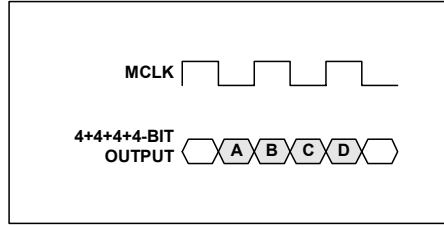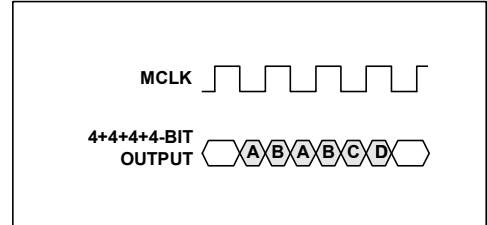

Figure 13 Output Data Formats (Modes 1, 3, 4)

Figure 14 Output Data Formats (Mode 2)

OUTPUT FORMAT	OUTPUT PINS	OUTPUT
4+4+4+4-bit (nibble)	OP[3:0]	A = d15, d14, d13, d12 B = d11, d10, d9, d8 C = d7, d6, d5, d4 D = d3, d2, d1, d0

Table 3 Details of Output Data Shown in Figure 13 and Figure 14

CONTROL INTERFACE

The internal control registers are programmable via the serial digital control interface. The register contents can be read back via the serial interface on pin OP[3]/SDO.

Note: It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values (as shown in Table 5).

SERIAL INTERFACE: REGISTER WRITE

Figure 15 shows register writing in serial mode. Three pins, SCK, SDI and SEN are used. A six-bit address (a5, 0, a3, a2, a1, a0) is clocked in through SDI, MSB first, followed by an eight-bit data word (b7, b6, b5, b4, b3, b2, b1, b0), also MSB first. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register. Note all valid registers have address bit a4 equal to 0 in write mode.
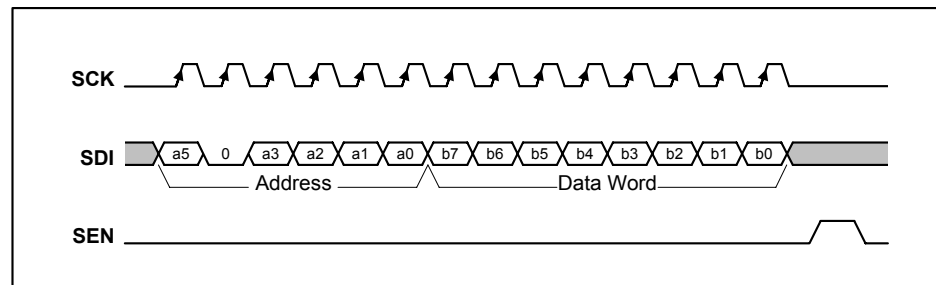
Figure 15 Serial Interface Register Write

A software reset is carried out by writing to Address "000100" with any value of data, (i.e. Data Word = XXXXXXXX.

SERIAL INTERFACE: REGISTER READ-BACK

Figure 16 shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit a4 set to 1, followed by an 8-bit dummy data word. Writing address (a5, 1, a3, a2, a1, a0) will cause the contents (d7, d6, d5, d4, d3, d2, d1, d0) of corresponding register (a5, 0, a3, a2, a1, a0) to be output MSB first on pin SDO (on the falling edge of SCK). Note that pin SDO is shared with an output pin, OP[3], so no data can be read when reading from a register. The next word may be read in to SDI while the previous word is still being output on SDO.
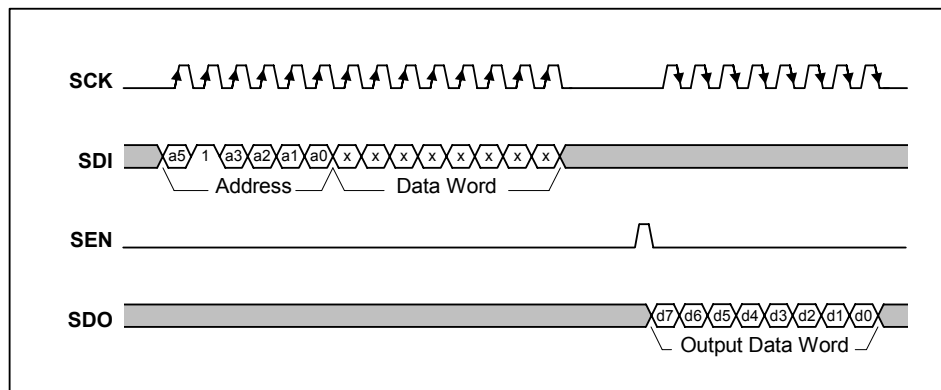
Figure 16 Serial Interface Register Read-back

TIMING REQUIREMENTS

To use this device a master clock (MCLK) of up to 24MHz and a per-pixel synchronisation clock (VSMP) of up to 12MHz are required. These clocks drive a timing control block, which produces internal signals to control the sampling of the video signal. MCLK to VSMP ratios and maximum sample rates for the various modes are shown in Table 4.

PROGRAMMABLE VSMP DETECT CIRCUIT

The VSMP input is used to determine the sampling point and frequency of the WM8152. Under normal operation a pulse of 1 MCLK period should be applied to VSMP at the desired sampling frequency (as shown in the Operating Mode Timing Diagrams) and the input sample will be taken on the first rising MCLK edge after VSMP has gone low. However, in certain applications such a signal may not be readily available. The programmable VSMP detect circuit in the WM8152 allows the sampling point to be derived from any signal of the correct frequency, such as a CCD shift register clock, when applied to the VSMP pin.

When enabled, by setting the VSMPDET control bit, the circuit detects either a rising or falling edge (determined by POSNNEG control bit) on the VSMP input pin and generates an internal VSMP pulse. This pulse can optionally be delayed by a number of MCLK periods, specified by the VDEL[2:0] bits. Figure 17 shows the internal VSMP pulses that can be generated by this circuit for a typical clock input signal. The internal VSMP pulse is then applied to the timing control block in place of the normal VSMP pulse provided from the input pin. The sampling point then occurs on the first rising MCLK edge after this internal VSMP pulse, as shown in the Operating Mode Timing Diagrams.

Figure 17 Internal VSMP Pulses Generated by Programmable VSMP Detect Circuit

REFERENCES

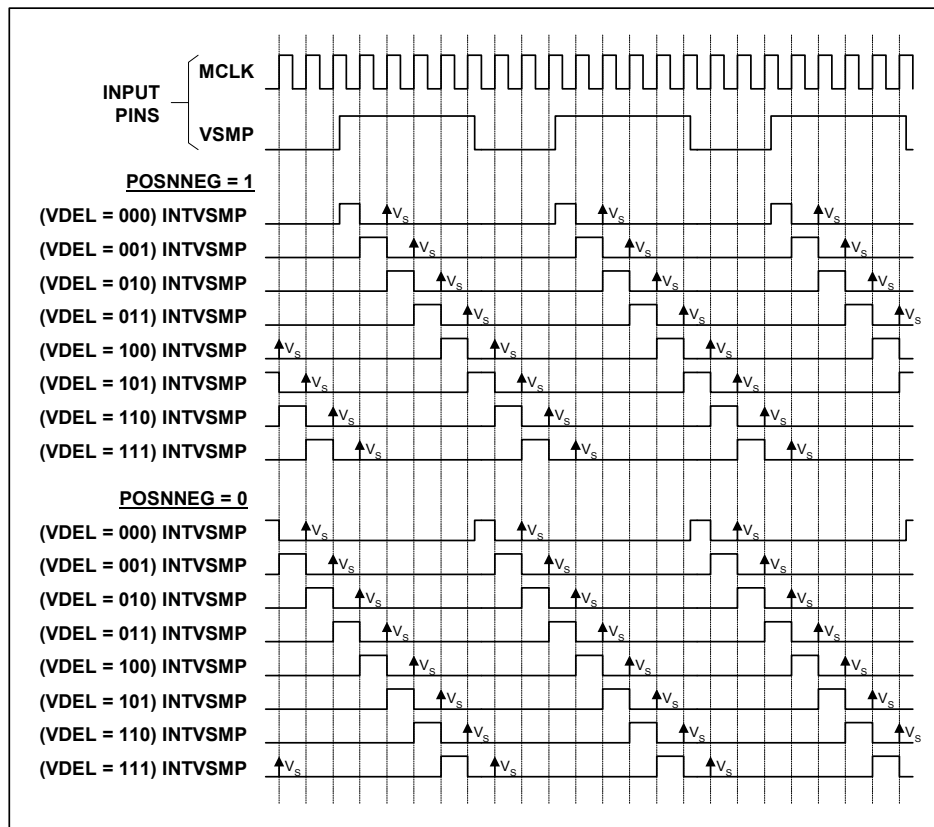The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins VRT and VRB, where they must be decoupled to ground. Pin VRX is driven by a similar buffer, and also requires decoupling. The output buffer from the RLCDAC also requires decoupling at pin VRLC/VBIAS when this is configured as an output.

POWER SUPPLY

The WM8152 can run from a 5V single supply or from split 5V (core) and 3.3V (digital interface) supplies.

POWER MANAGEMENT

Power management for the device is performed via the Control Interface. The device can be powered on or off completely by setting the EN bit low.

All the internal registers maintain their previously programmed value in power down mode and the Control Interface inputs remain active.

OPERATING MODES

Table 4 summarises the most commonly used modes, the clock waveforms required and the register contents required for CDS and non-CDS operation.

MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	TIMING REQUIREMENTS	REGISTER CONTENTS WITH CDS	REGISTER CONTENTS WITHOUT CDS
1	Monochrome/ Colour Line-by-Line	Yes	4MSPS	MCLK max = 24MHz MCLK:VSMP ratio is 6:1	SetReg1: 0F(hex)	SetReg1: 0D(hex)
2	Fast Monochrome/ Colour Line-by-Line	Yes	8MSPS	MCLK max = 24MHz MCLK:VSMP ratio is 3:1	Identical to Mode 1 plus SetReg3: bits 5:4 must be set to 0(hex)	Identical to Mode 1
3	Maximum speed Monochrome/ Colour Line-by-Line	No	12MSPS	MCLK max = 24MHz MCLK:VSMP ratio is 2:1	CDS not possible	SetReg1: 4D(hex)
4	Slow Monochrome/ Colour Line-by-Line	Yes	3MSPS	MCLK max = 24MHz MCLK:VSMP ratio is 2n:1, n $\geq$ 4	Identical to Mode 1	Identical to Mode 1

Table 4 WM8152 Operating Modes

OPERATING MODE TIMING DIAGRAMS

The following diagrams show 4-bit multiplexed output data and MCLK, VSMP and input video requirements for operation of the most commonly used modes as shown in Table 4. The diagrams are identical for both CDS and non-CDS operation.
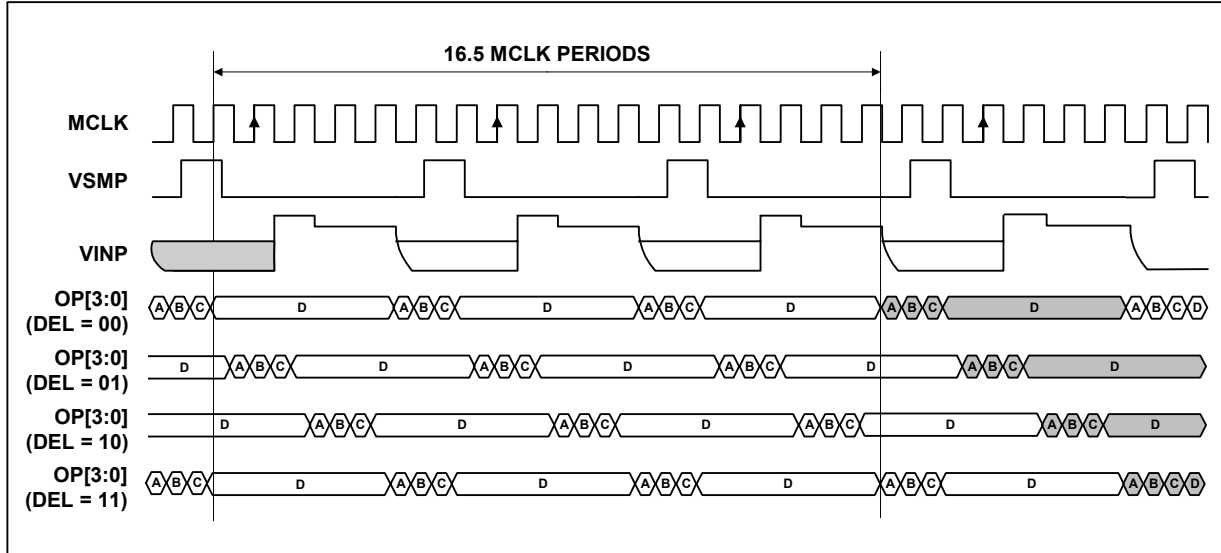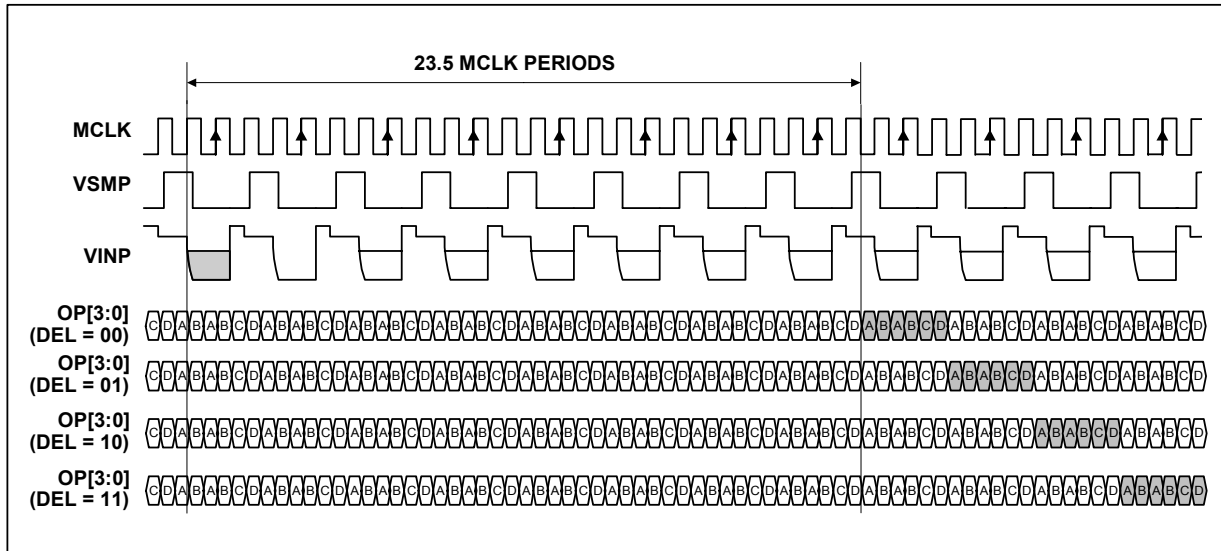

Figure 18 Mode 1 Operation
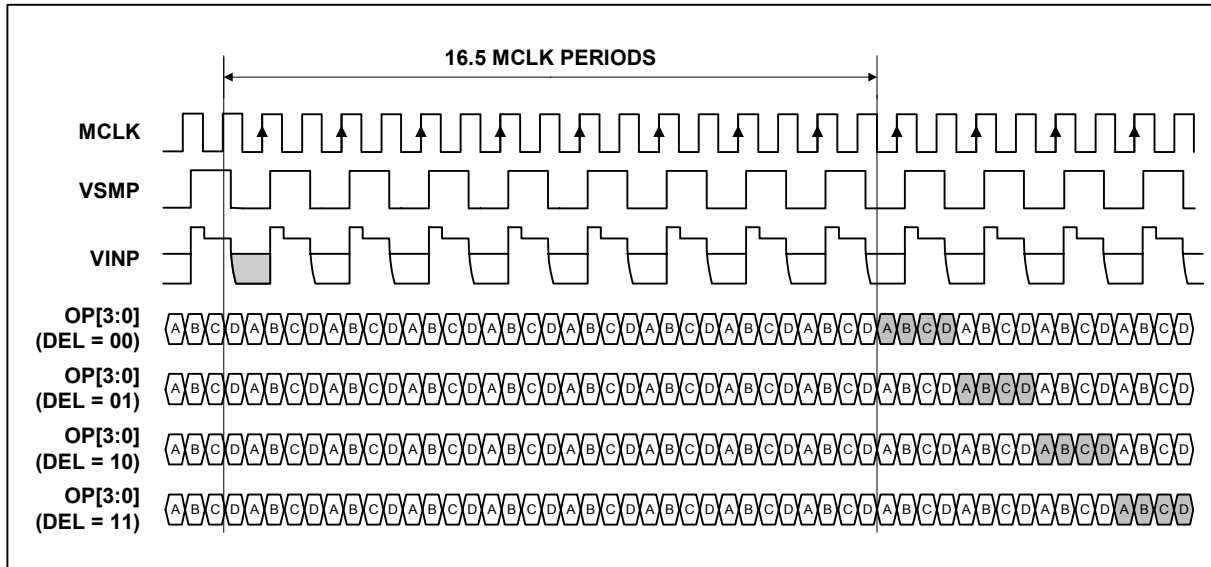

Figure 19 Mode 2 Operation
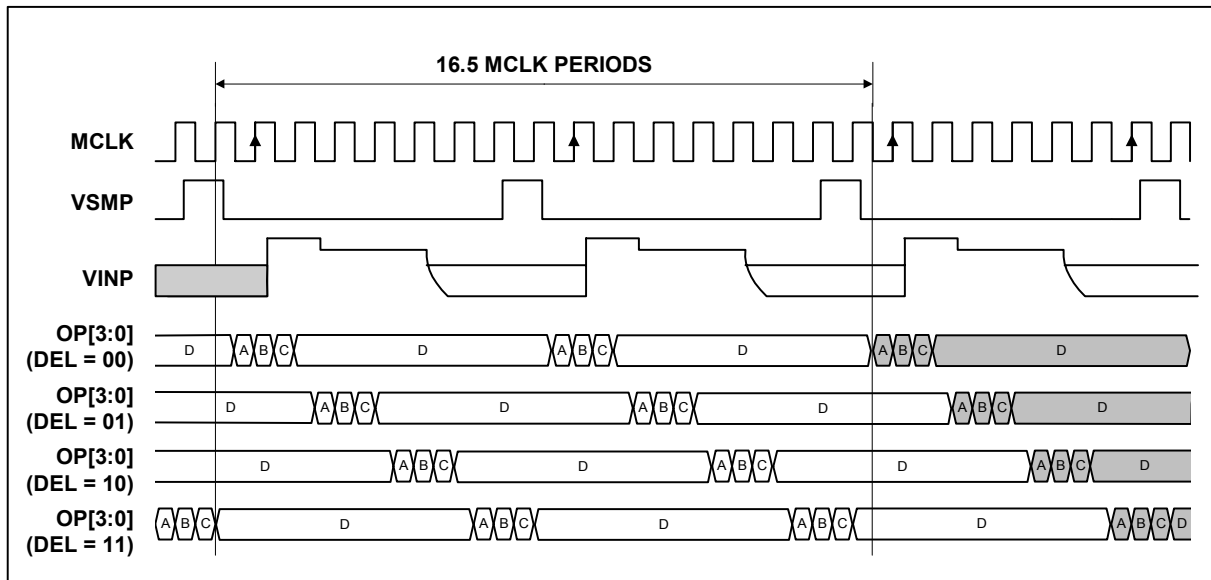
Figure 20 Mode 3 Operation

Figure 21 Mode 4 Operation (MCLK:VSMP Ratio = 8:1)

DEVICE CONFIGURATION

REGISTER MAP

The following table describes the location of each control bit used to determine the operation of the WM8152. The register map is programmed by writing the required codes to the appropriate addresses via the serial interface.

ADDRESS	DESCRIPTION	DEF	RW	BIT							
<a5:a0>		(hex)		b7	b6	b5	b4	b3	b2	b1	b0
000001	Setup Reg 1	0F	RW	0	MODE3	PGAFS[1]	PGAFS[0]	1	1	CDS	EN
000010	Setup Reg 2	23	RW	DEL[1]	DEL[0]	RLCDACRNG	0	VRLCEXT	INVOP	1	1
000011	Setup Reg 3	1F	RW	0	0	CDSREF [1]	CDSREF [0]	RLCV[3]	RLCV[2]	RLCV[1]	RLCV[0]
000100	Software Reset	00	W								
000110	Setup Reg 4	05	RW	0	0	INTM[1]	INTM[0]	RLCINT	1	0	1
000111	Revision Number	41	R	0	1	0	0	0	0	0	1
001000	Setup Reg 5	00	RW	0	0	0	POSNNEG	VDEL[2]	VDEL[1]	VDEL[0]	VSMPDET
001001	Test Reg 1	00	RW	TCLK	0	0	0	0	0	0	0
001010	Reserved	00	RW	0	0	0	0	0	0	0	0
001011	Reserved	00	RW	0	0	0	0	0	0	0	0
001100	Reserved	00	RW	0	0	0	0	0	0	0	0
100000	DAC Value (Red)	80	RW	DACR[7]	DACR[6]	DACR[5]	DACR[4]	DACR[3]	DACR[2]	DACR[1]	DACR[0]
100001	DAC Value (Green)	80	RW	DACG[7]	DACG[6]	DACG[5]	DACG[4]	DACG[3]	DACG[2]	DACG[1]	DACG[0]
100010	DAC Value (Blue)	80	RW	DACB[7]	DACB[6]	DACB[5]	DACB[4]	DACB[3]	DACB[2]	DACB[1]	DACB[0]
100011	DAC Value (RGB)	80	W	DAC[7]	DAC[6]	DAC[5]	DAC[4]	DAC[3]	DAC[2]	DAC[1]	DAC[0]
101000	PGA Gain (Red)	00	RW	PGAR[7]	PGAR[6]	PGAR[5]	PGAR[4]	PGAR[3]	PGAR[2]	PGAR[1]	PGAR[0]
101001	PGA Gain (Green)	00	RW	PGAG[7]	PGAG[6]	PGAG[5]	PGAG[4]	PGAG[3]	PGAG[2]	PGAG[1]	PGAG[0]
101010	PGA Gain (Blue)	00	RW	PGAB[7]	PGAB[6]	PGAB[5]	PGAB[4]	PGAB[3]	PGAB[2]	PGAB[1]	PGAB[0]
101011	PGA Gain (RGB)	00	W	PGA[7]	PGA[6]	PGA[5]	PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]

Table 5 Register Map

REGISTER MAP DESCRIPTION

The following table describes the function of each of the control bits shown in Table 5.

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Setup Register 1	0	EN	1	0 = complete power down, 1 = fully active.
	1	CDS	1	Select correlated double sampling mode: 0 = single ended mode, 1 = CDS mode.
	3:2	Reserved	11	Must be set to one
	5:4	PGAFS[1:0]	00	Offsets PGA output to optimise the ADC range for different polarity sensor output signals. Zero differential PGA input signal gives: 00 = Zero output 10 = Full-scale positive output (use for bipolar video) (use for negative going video) 01 = Zero output 11 = Full-scale negative output (use for positive going video)
	6	MODE3	0	Required when operating in MODE3: 0 = other modes, 1 = MODE3.
	7	Reserved	0	Must be set to zero
Setup Register 2	1:0	Reserved	11	Must be set to one
	2	INVOP	0	Digitally inverts the polarity of output data. 0 = negative going video gives negative going output, 1 = negative-going video gives positive going output data.
	3	VRLCEXT	0	When set powers down the RLCDAC, changing its output to Hi-Z, allowing VRLC/VBIAS to be externally driven.
	4	Reserved	0	Must be set to zero
	5	RLCDACRNG	1	Sets the output range of the RLCDAC. 0 = RLCDAC ranges from 0 to VDD (approximately), 1 = RLCDAC ranges from 0 to VRT (approximately).
	7:6	DEL[1:0]	00	Sets the output latency in ADC clock periods. 1 ADC clock period = 2 MCLK periods except in Mode 2 where 1 ADC clock period = 3 MCLK periods. 00 = Minimum latency 10 = Delay by two ADC clock periods 01 = Delay by one ADC clock 11 = Delay by three ADC clock period periods
Setup Register 3	3:0	RLCV[3:0]	1111	Controls RLCDAC driving VRLC pin to define single ended signal reference voltage or Reset Level Clamp voltage. See Electrical Characteristics section for ranges.
	5:4	CDSREF[1:0]	01	CDS mode reset timing adjust. 00 = Advance 1 MCLK period 10 = Retard 1 MCLK period 01 = Normal 11 = Retard 2 MCLK periods
	7:6	Reserved	00	Must be set to zero
Software Reset				Any write to Software Reset causes all cells to be reset. It is recommended that a software reset be performed after a power-up before any other register writes.
Setup Register 4	2:0	Reserved	101	Must be set to 101
	3	RLCINT	0	This bit is used to determine whether Reset Level Clamping is enabled. 0 = RLC disabled, 1 = RLC enabled.
	5:4	INTM[1:0]	00	Colour selection bits used in internal modes. 00 = Red, 01 = Green, 10 = Blue and 11 = Reserved. See Table 2 for details.
	7:6	Reserved	00	Must be set to zero

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Setup Register 5	0	VSMPDET	0	0 = Normal operation, signal on VSMP input pin is applied directly to Timing Control block. 1 = Programmable VSMP detect circuit is enabled. An internal synchronisation pulse is generated from signal applied to VSMP input pin and is applied to Timing Control block.
	3:1	VDEL[2:0]	000	When VSMPDET = 0 these bits have no effect. When VSMPDET = 1 these bits set a programmable delay from the detected edge of the signal applied to the VSMP pin. The internally generated pulse is delayed by VDEL MCLK periods from the detected edge. See Figure 17, Internal VSMP Pulses Generated for details.
	4	POSNNEG	0	When VSMPDET = 0 this bit has no effect. When VSMPDET = 1 this bit controls whether positive or negative edges are detected: 0 = Negative edge on VSMP pin is detected and used to generate internal timing pulse. 1 = Positive edge on VSMP pin is detected and used to generate internal timing pulse. See Figure 17 for further details.
	7:5	Reserved	000	Must be set to zero
Test Register 1	7	TCLK	0	0 = Normal Operation, OP[3:0] output ADC data. 1 = Internal Clock Test Mode. This allows internal timing signals to be multiplexed onto the OP[3:0] pins as follows.

PIN	TCLK=0	TCLK=1
OP[3]	OP[3]	INTVSMP
OP[2]	OP[2]	Video sample clock
OP[1]	OP[1]	ADC clock
OP[0]	OP[0]	Reset sample clock

REGISTER	BIT NO	BIT NAME(S)	DEFAULT	DESCRIPTION
Offset DAC (Red)	7:0	DACR[7:0]	10000000	Red channel offset DAC value. Used under control of the INTM[1:0] control bits.
Offset DAC (Green)	7:0	DACG[7:0]	10000000	Green channel offset DAC value. Used under control of the INTM[1:0] control bits.
Offset DAC (Blue)	7:0	DACB[7:0]	10000000	Blue channel offset DAC value. Used under control of the INTM[1:0] control bits.
Offset DAC (RGB)	7:0	DAC[7:0]		A write to this register location causes the red, green and blue offset DAC registers to be overwritten by the new value
PGA gain (Red)	7:0	PGAR[7:0]	00000000	Determines the gain of the red channel PGA according to the equation: Red channel PGA gain = $[0.78+(\text{PGAR}[7:0]*7.57)/255]$. Used under control of the INTM[1:0] control bits.
PGA gain (Green)	7:0	PGAG[7:0]	00000000	Determines the gain of the green channel PGA according to the equation: Green channel PGA gain = $[0.78+(\text{PGAG}[7:0]*7.57)/255]$. Used under control of the INTM[1:0] control bits.
PGA gain (Blue)	7:0	PGAB[7:0]	00000000	Determines the gain of the blue channel PGA according to the equation: Blue channel PGA gain = $[0.78+(\text{PGAB}[7:0]*7.57)/255]$. Used under control of the INTM[1:0] control bits.
PGA gain (RGB)	7:0	PGA[7:0]		A write to this register location causes the red, green and blue PGA gain registers to be overwritten by the new value

Table 6   Register Control Bits

APPLICATIONS INFORMATION
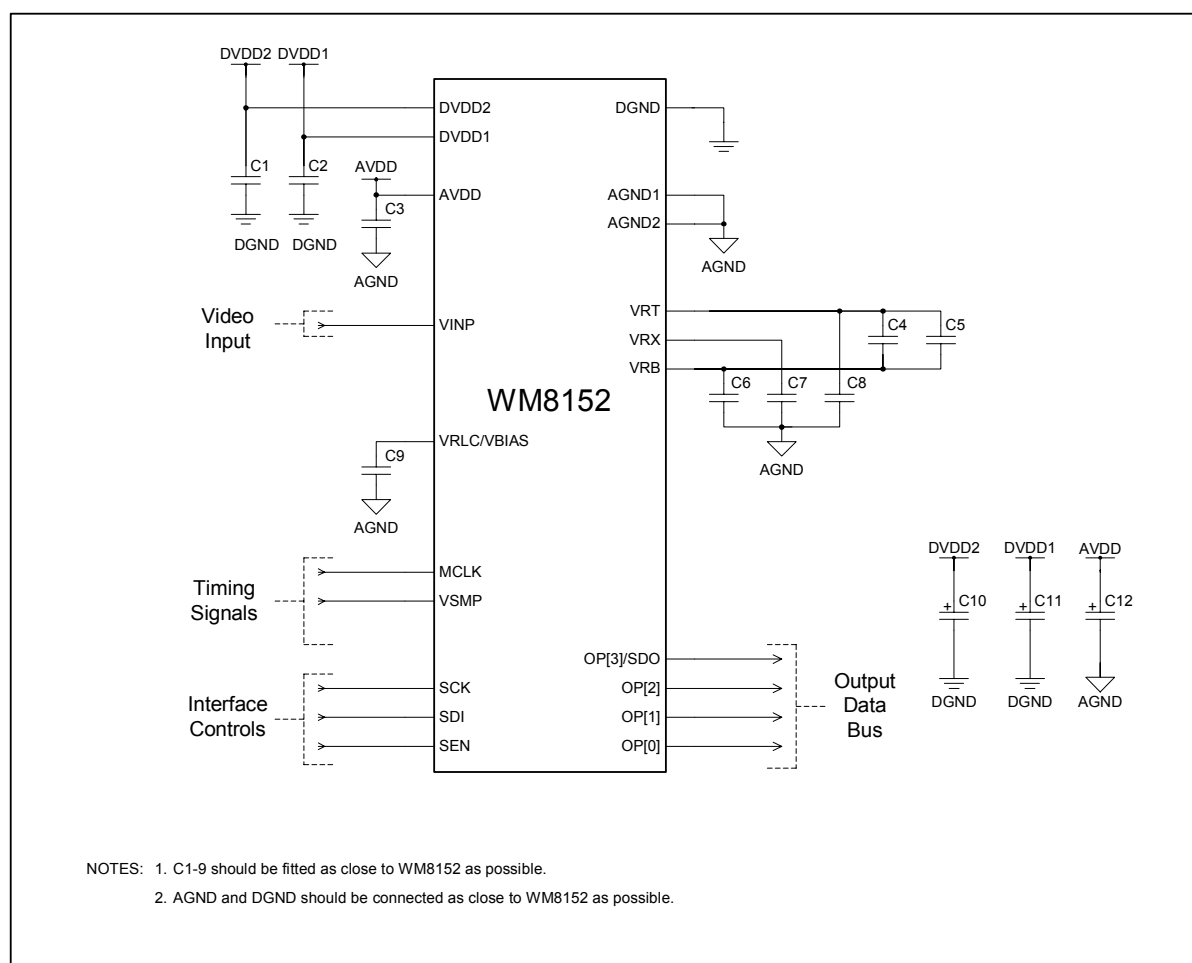
RECOMMENDED EXTERNAL COMPONENTS

Figure 22 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1	100nF	De-coupling for DVDD2.
C2	100nF	De-coupling for DVDD1.
C3	100nF	De-coupling for AVDD.
C4	10nF	High frequency de-coupling between VRT and VRB.
C5	1µF	Low frequency de-coupling between VRT and VRB (non-polarised).
C6	100nF	De-coupling for VRB.
C7	100nF	De-coupling for VRX.
C8	100nF	De-coupling for VRT.
C9	100nF	De-coupling for VRLC.
C10	10µF	Reservoir capacitor for DVDD2.
C11	10µF	Reservoir capacitor for DVDD1.
C12	10µF	Reservoir capacitor for AVDD.

Table 7 External Components Descriptions

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm)   **DM0015.C**
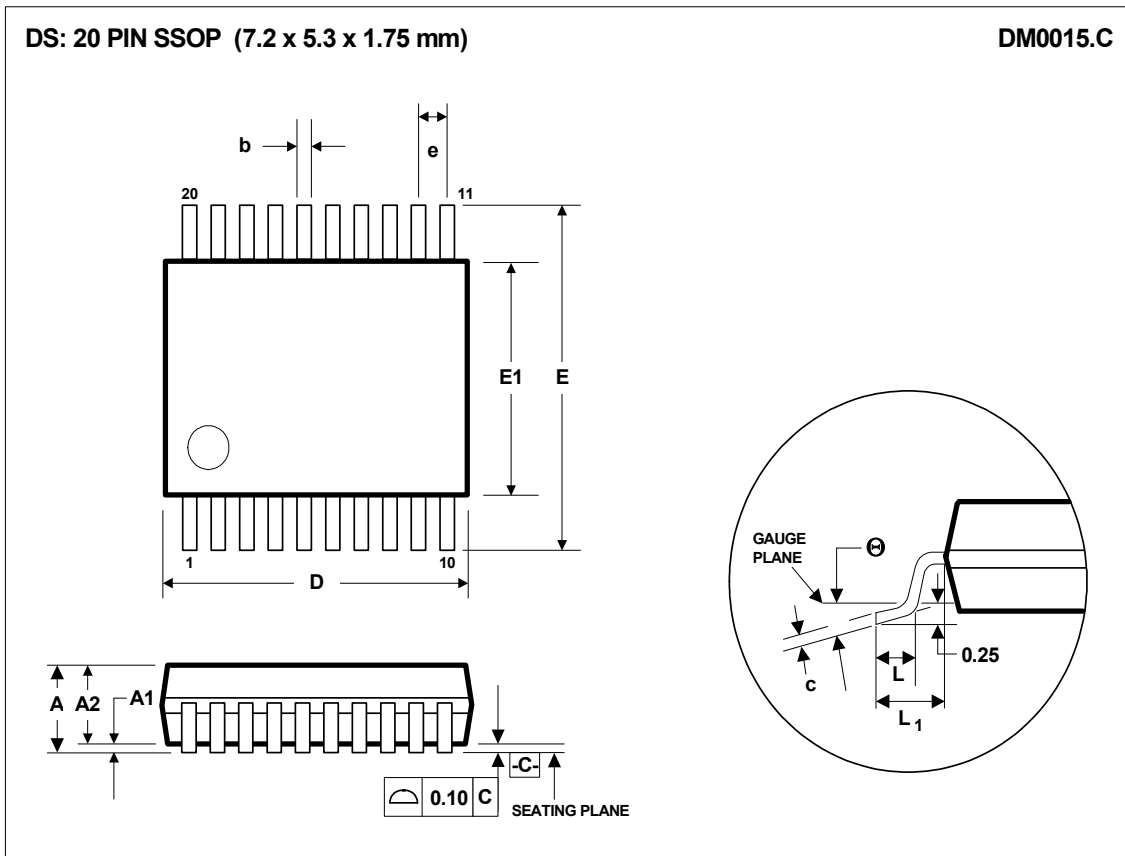
Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	2.0
A₁	0.05	-----	-----
A₂	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e	0.65 BSC		
E	7.40	7.80	8.20
E₁	5.00	5.30	5.60
L	0.55	0.75	0.95
L₁	1.25 REF		
θ	0°	4°	8°
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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ADDRESS:

Wolfson Microelectronics plc

20 Bernard Terrace

Edinburgh

EH8 9NX

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com