

NP60N04VUK

MOS FIELD EFFECT TRANSISTOR

R07DS0576EJ0100 Rev.1.00 Nov 24, 2011

Description

The NP60N04VUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

• Super low on-state resistance

 $R_{DS(on)} = 3.85 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 30 \text{ A})$

- Low C_{iss} : $C_{iss} = 2450 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

| Part No. | Lead Plating | Pac | Package | |
|---------------------|---------------|------------------|------------------|-----------------|
| NP60N04VUK-E1-AY *1 | Pure Sn (Tin) | Tape 2500 p/reel | Taping (E1 type) | TO-252 (MP-3ZP) |
| NP60N04VUK-E2-AY *1 | | | Taping (E2 type) | |

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

| Item | Symbol | Ratings | Unit |
|---|-----------------------|------------|------|
| Drain to Source Voltage (V _{GS} = 0 V) | V _{DSS} | 40 | V |
| Gate to Source Voltage (V _{DS} = 0 V) | V _{GSS} | ±20 | V |
| Drain Current (DC) (T _C = 25°C) | I _{D(DC)} | ±60 | А |
| Drain Current (pulse) *1 | I _{D(pulse)} | ±240 | А |
| Total Power Dissipation (T _C = 25°C) | P _{T1} | 105 | W |
| Total Power Dissipation (T _A = 25°C) | P _{T2} | 1.2 | W |
| Channel Temperature | T _{ch} | 175 | °C |
| Storage Temperature | T _{stg} | -55 to 175 | °C |
| Repetitive Avalanche Current *2 | I _{AR} | 28 | А |
| Repetitive Avalanche Energy *2 | E _{AR} | 78 | mJ |

Notes: *1 $\,T_{C}$ = 25°C, $P_{W} \leq$ 10 $\mu s,\, Duty\,\, Cycle \leq$ 1%

Thermal Resistance

^{*2} R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

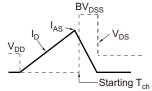
Electrical Characteristics (T_A = 25°C)

| Item | Symbol | MIN. | TYP. | MAX. | Unit | Test Conditions | |
|--|---------------------|------|------|------|------|---|--|
| Zero Gate Voltage Drain Current | I _{DSS} | _ | _ | 1 | μΑ | $V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$ | |
| Gate Leakage Current | I _{GSS} | _ | _ | ±100 | nA | $V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$ | |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | V | $V_{DS} = V_{GS}, I_{D} = 250 \mu A$ | |
| Forward Transfer Admittance *1 | y _{fs} | 22 | 44 | _ | S | $V_{DS} = 5 \text{ V}, I_{D} = 30 \text{ A}$ | |
| Drain to Source On-state Resistance *1 | R _{DS(on)} | _ | 3.20 | 3.85 | mΩ | $V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$ | |
| Input Capacitance | C _{iss} | _ | 2450 | 3680 | pF | V _{DS} = 25 V | |
| Output Capacitance | Coss | _ | 340 | 510 | pF | $V_{GS} = 0 V$ | |
| Reverse Transfer Capacitance | C _{rss} | _ | 140 | 260 | pF | f = 1 MHz | |
| Turn-on Delay Time | t _{d(on)} | _ | 19 | 50 | ns | $V_{DD} = 20 \text{ V}, I_D = 30 \text{ A}$ | |
| Rise Time | t _r | _ | 9 | 30 | ns | V _{GS} = 10 V | |
| Turn-off Delay Time | t _{d(off)} | _ | 45 | 90 | ns | $R_G = 0 \Omega$ | |
| Fall Time | t _f | _ | 7 | 20 | ns | | |
| Total Gate Charge | Q_{G} | _ | 42 | 63 | nC | V _{DD} = 32 V | |
| Gate to Source Charge | Q _{GS} | _ | 11 | _ | nC | V _{GS} = 10 V | |
| Gate to Drain Charge | Q_{GD} | _ | 11 | _ | nC | $I_D = 60 \text{ A}$ | |
| Body Diode Forward Voltage *1 | $V_{F(S-D)}$ | _ | 0.9 | 1.5 | V | I _F = 60 A, V _{GS} = 0 V | |
| Reverse Recovery Time | t _{rr} | _ | 44 | _ | ns | I _F = 60 A, V _{GS} = 0 V | |
| Reverse Recovery Charge | Q _{rr} | _ | 40 | _ | nC | di/dt = 100 A/μs | |

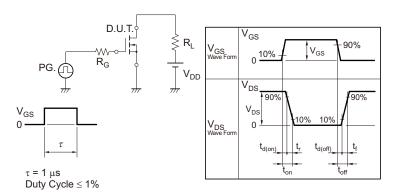
Note: *1 Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{GS} = 20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD} V_{DD} V_{DD}



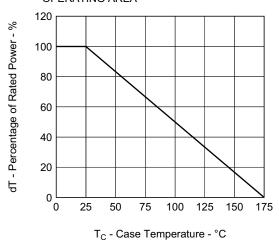
TEST CIRCUIT 2 SWITCHING TIME



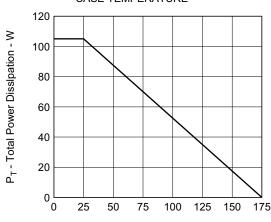
TEST CIRCUIT 3 GATE CHARGE

Typical Characteristics $(T_A = 25^{\circ}C)$

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

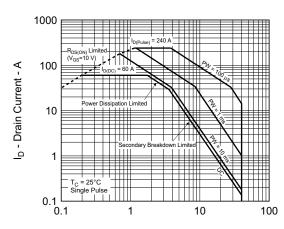


TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



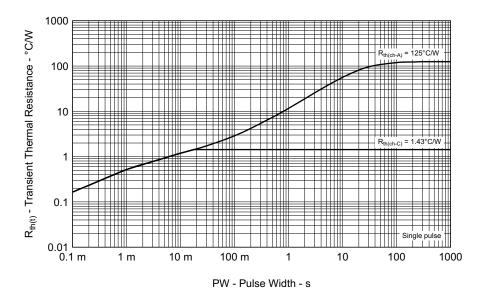
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



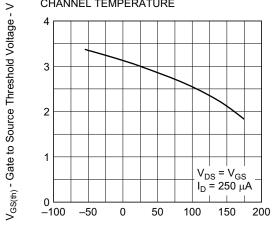
 V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



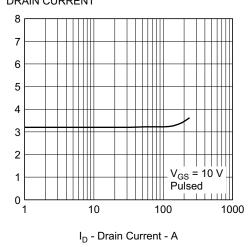
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE 300 250 I_D - Drain Current - A 200 150 100 50 V_{GS} = 10 V Pulsed 0 0.2 0 0.4 0.6 8.0 1.0 V_{DS} - Drain to Source Voltage - V



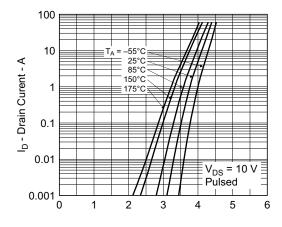


 T_{ch} - Channel Temperature - $^{\circ}C$

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

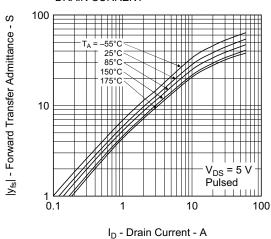


FORWARD TRANSFER CHARACTERISTICS

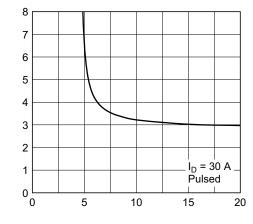


V_{GS} - Gate to Source Voltage - V

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



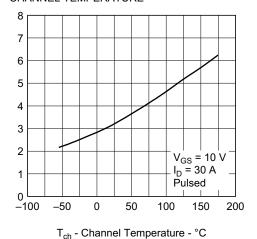
V_{GS} - Gate to Source Voltage - V

 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

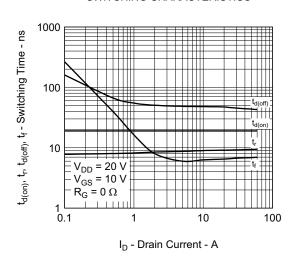
 $R_{\text{DS(on)}}$ - Drain to Source On-State Resistance - $m\Omega$

 $R_{DS(on)}$ - Drain to Source On-State Resistance - $m\Omega$

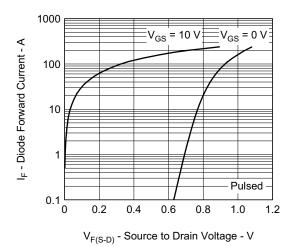
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



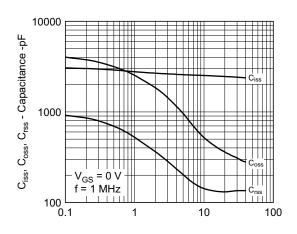
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

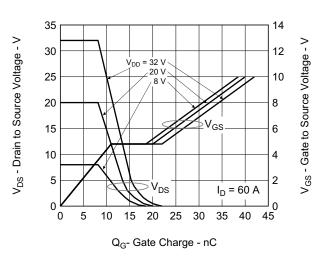


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

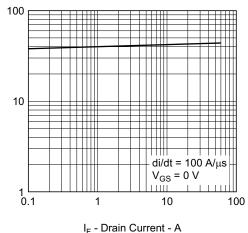


V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



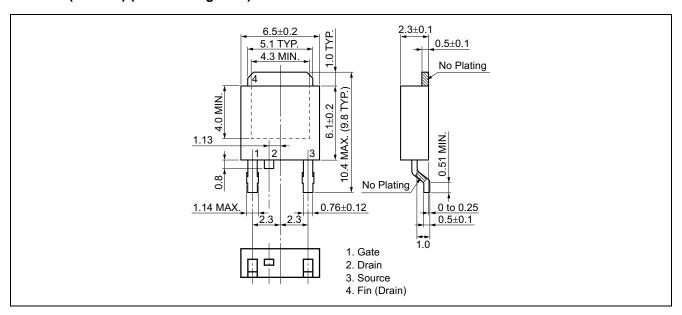
REVERSE RECOVERY TIME vs. **DRAIN CURRENT**



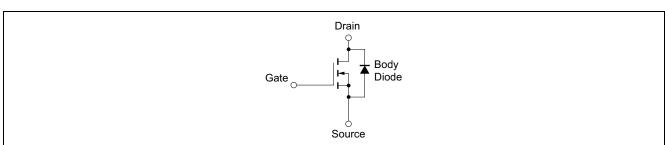
t_{rr} - Reverse Recovery Time - ns

Package Drawing (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)



Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP60N04VUK Data Sheet

| | | Description | | |
|------|--------------|-------------|----------------------|--|
| Rev. | Date | Page | Summary | |
| 1.00 | Nov 24, 2011 | _ | First Edition Issued | |

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