DS14185 EIA/TIA-232 3 Driver x 5 Receiver

Check for Samples: DS14185

FEATURES

- **Replaces One 1488 and Two 1489s**
- **Conforms to EIA/TIA-232-E**
- **3 Drivers and 5 Receivers**
- **Flow Through Pinout**
- **Failsafe Receiver Outputs**
- **20-pin SOIC Package**
- **LapLink Compatible −200 kbps Data Rate**

DESCRIPTION

The DS14185 is a three driver, five receiver device which conforms to the EIA/TIA-232-E standard.

The flow-through pinout facilitates simple non-crossover board layout. The DS14185 provides a one-chip solution for the common 9-pin serial RS-232 interface between data terminal and data communications equipment.

Connection Diagram

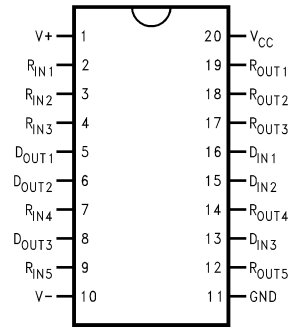


Figure 1. SOIC
See Package DW0020B

Functional Diagram

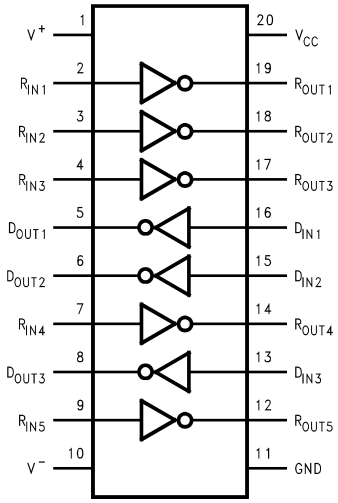


Figure 2.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})		+7V
Supply Voltage (V^+)		+15V
Supply Voltage (V^-)		−15V
Driver Input Voltage		0V to V_{CC}
Driver Output(3) Voltage (Power Off)		±15V
Receiver Input Voltage		±25V
Receiver Output Voltage (R_{OUT})		0V to V_{CC}
Maximum Package Power Dissipation @ +25°C	DW Package	1488 mW
Derate DW Package		11.9 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range (Soldering, 4 seconds)		+260°C
ESD Ratings (HBM, 1.5 kΩ, 100 pF)		≥1.5 kV

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be specified. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Only one driver output shorted at a time.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V^+)	+9.0	+12.0	+13.2	V
Supply Voltage (V^-)	−13.2	−12.0	−9.0	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics(1)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ(2)	Max	Units
DEVICE CHARACTERISTICS							
I_{CC}	V_{CC} Supply Current	No Load, All Inputs at +5V			21.0	30	mA
I^+	V^+ Supply Current(1)	No Load, All Driver Inputs at 0.8V or +2V All Receiver Inputs at 0.8V or 2.4V.	V^+ = 9V, V^- = −9V		8.7	15	mA
			V^+ = 13.2V, V^- = −13.2V		13	22	mA
I^-	V^- Supply Current(1)		V^+ = 9V, V^- = −9V		−12.5	−22	mA
			V^+ = 13.2V, V^- = −13.2V		−16.5	−28	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if −6V is a maximum, the typical value (−6.8V) is more negative.
(2) All typicals are given for: V_{CC} = +5.0V, V^+ = +12.0V, V^- = −12V, T_A = +25°C.

Electrical Characteristics[1] (continued)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Units
DRIVER CHARACTERISTICS						
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current[3]	V_{IN} = 5V			10	µA
I_{IL}	Low Level Input Current[3]	V_{IN} = 0V		−1.24	−1.5	mA
V_{OH}	High Level Output Voltage[3]	R_L = 3 kΩ, V_{IN} = 0.8V, V^+ = 9V, V^- = −9V	6	7		V
		R_L = 3 kΩ, V_{IN} = 0.8V, V^+ = +12V, V^- = −12V	8.5	9		V
		R_L = 7 kΩ, V_{IN} = 0.8V, V^+ = +13.2V, V^- = −13.2V	10	11.5		V
V_{OL}	Low Level Output Voltage[3]	R_L = 3 kΩ, V_{IN} = 2V, V^+ = 9V, V^- = −9V		−7	−6	V
		R_L = 3 kΩ, V_{IN} = 2V, V^+ = +12V, V^- = −12V		−8	−7.5	V
		R_L = 7 kΩ, V_{IN} = 0.8V, V^+ = +13.2V, V^- = −13.2V		−11	−10	V
I_{OS}+	Output High Short Circuit Current[3]	V_O = 0V, V_{IN} = 0.8V	−6	−13	−18	mA
I_{OS}−	Output Low Short Circuit Current[3]	V_O = 0V, V_{IN} = 2.0V	6	13	18	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V^+ = V^- = V_{CC} = 0V	300			Ω
		−2V ≤ V_O ≤ +2V, V^+ = V^- = V_{CC} = Open Ckt	300			Ω
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold (Recognized as a High Signal)	V_O ≤ 0.4V, I_O = 3.2 mA		1.85	2.4	V
V_{TL}	Input Low Threshold (Recognized as a Low Signal)	V_O ≥ 2.5V, I_O = −0.5 mA	0.7	1.0		V
R_{IN}	Input Resistance	V_{IN} = ±3V to ±15V	3.0	4.1	7.0	kΩ
I_{IN}	Input Current[3]	V_{IN} = +15V	2.1	4.1	5.0	mA
		V_{IN} = +3V	0.43	0.7	1	mA
		V_{IN} = −15V	−5.0	−4.1	−2.1	mA
		V_{IN} = −3V	−1	−0.65	−0.43	mA
V_{OH}	High Level Output Voltage[4]	I_{OH} = −0.5 mA, V_{IN} = −3V	2.6	4		V
		I_{OH} = −10 µA, V_{IN} = −3V	4.0	4.9		V
		I_{OH} = −0.5 mA, V_{IN} = Open Circuit	2.6	4		V
		I_{OH} = −10 µA, V_{IN} = Open Circuit	4.0	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 3.2 mA, V_{IN} = +3V		0.2	0.4	V
I_{OSR}	Short Circuit Current[3]	V_O = 0V, V_{IN} = 0V	−4	−2.7	−1.7	mA

(3) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if −6V is a maximum, the typical value (−6.8V) is more negative.

(4) If receiver inputs are unconnected, receiver output is a logic high.

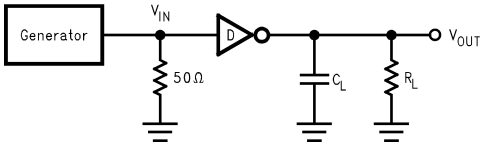
Switching Characteristics(1)

T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ(2)	Max	Units
DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	R_L = 3 kΩ, C_L = 50 pF (Figure 3 Figure 4)		60	350	ns
t_{PLH}	Propagation Delay Low to High			240	350	ns
t_r, t_f	Output Slew Rate(3)			50		ns
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	R_L = 1.5 kΩ, C_L = 15 pF (includes fixture plus probe), (Figure 5 Figure 6)		150	350	ns
t_{PLH}	Propagation Delay Low to High			240	350	ns
t_r	Rise Time			87	175	ns
t_f	Fall Time			40	100	ns

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if −6V is a maximum, the typical value (−6.8V) is more negative.
(2) All typicals are given for: V_{CC} = +5.0V, V^+ = +12.0V, V^- = −12V, T_A = +25°C.
(3) Refer to typical curves. Driver output slew rate is measured from the +3.0V to the −3.0V level on the output waveform. Inputs not under test are connected to V_{CC} or GND. Slew rate is determined by load capacitance. To comply with a 30 V/µs maximum slew rate, a minimum load capacitance of 390 pF is recommended.

Parameter Measurement Information



Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), t_r = t_f < 10 ns, V_{IH} = 3V, V_{IL} = 0V, duty cycle = 50%.

Figure 3. Driver Propagation Delay and Transition Time Test Circuit

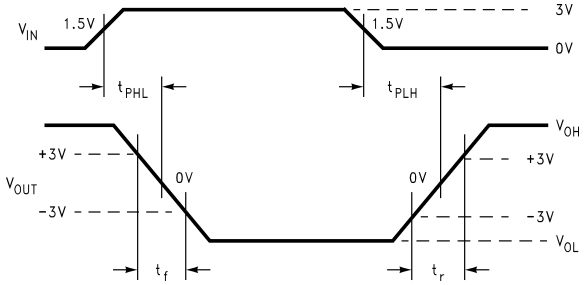
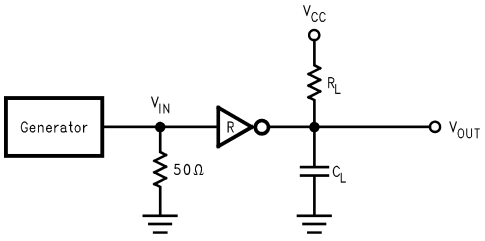


Figure 4. Driver Propagation Delay and Transition Time Waveforms Slew Rate (SR) = 6V/(t_r or t_f)



Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), t_r = t_f = 200 ns, V_{IH} = 3V, V_{IL} = −3V, duty cycle = 50%.

Figure 5. Receiver Propagation Delay and Transition Time Test Circuit

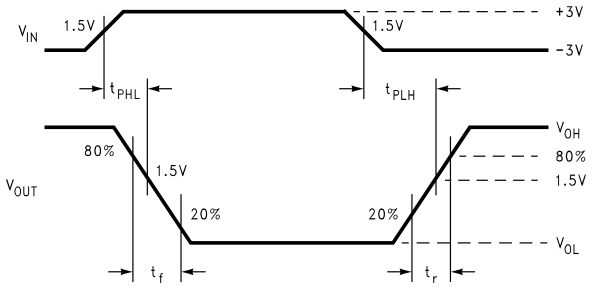


Figure 6. Receiver Propagation Delay and Transition Time Waveform

PIN DESCRIPTIONS

Pin #	Name	Description
13, 15, 16	D_{IN}	Driver Input Pins
5, 6, 8	D_{OUT}	Driver Output Pins, RS-232 Levels
2, 3, 4, 7, 9	R_{IN}	Receiver Input Pins, RS-232 Levels
12, 14, 17, 18, 19	R_{OUT}	Receiver Output Pins
11	GND	Ground
1	V^+	Positive Power Supply Pin ($+9.0 \le V^+ \le +13.2$)
10	V^-	Negative Power Supply Pin ($-9.0 \le V^- \le -13.2$)
20	V_{CC}	Positive Power Supply Pin (+5V ±5%)

APPLICATIONS INFORMATION

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD. The control lines are RTS, DTR, DSR, DCD, CTS, and RI.

The DS14185 is a 3 x 5 Driver/Receiver and offers a single chip solution for this DTE interface. As shown in Figure 7, this interface allows for direct flow-thru interconnect. For a more conservative design, the user may wish to insert ground traces between the signal lines to minimize cross talk.

LapLink COMPATIBILITY

The DS14185 can easily provide 128 kbps data rate under maximum driver load conditions of C_L = 2500 pF and R_L = 3 kΩ, while power supplies are:

V_{CC} = 4.75V, V^+ = 10.8V, V^- = −10.8V (1)

MOUSE DRIVING

A typical mouse can be powered from the drivers. Two driver outputs connected in parallel and set to V_{OH} can be used to supply power to the V^+ pin of the mouse. The third driver output is set to V_{OL} to sink the current from the V^- terminal. Refer to typical curves of V_{OUT}/I_{OUT}.Typical mouse specifications are:

10 mA at +6V (2)

5 mA at −6V (3)

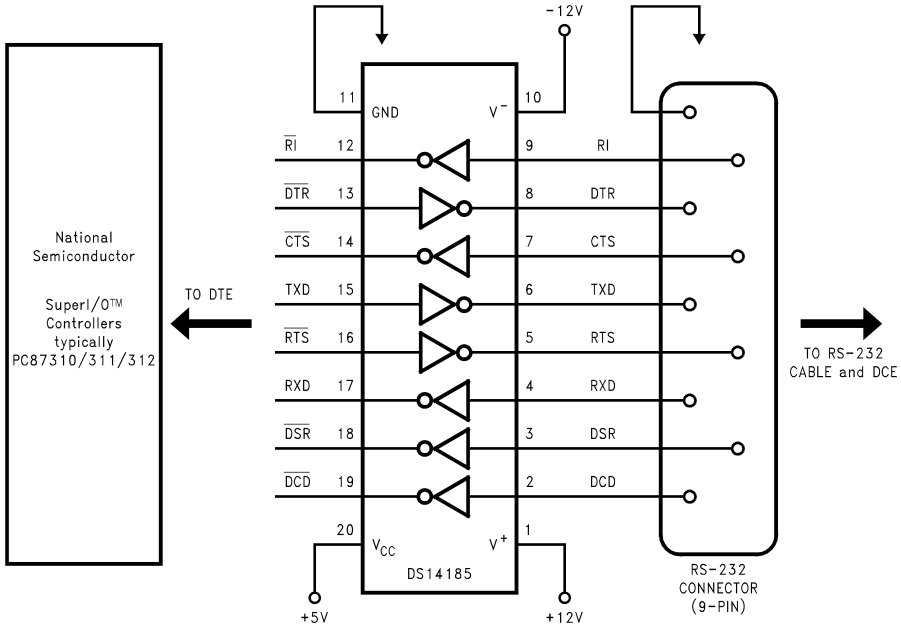


Figure 7. Typical DTE Application

Typical Performance Characteristics

The below input waveforms were used to generate all Typical AC Characteristics.

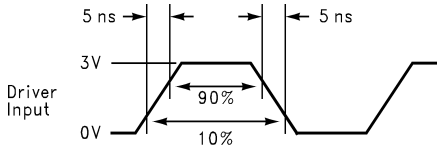


Figure 8.

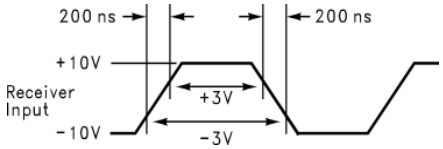


Figure 9.

Driver Output Slew Rate between +3V and −3V vs Load Capacitance
Conditions: V_{CC} = 5V, R_L = 5 kΩ, T_A = 25°C, f_{IN} = 64 kHz Square Wave

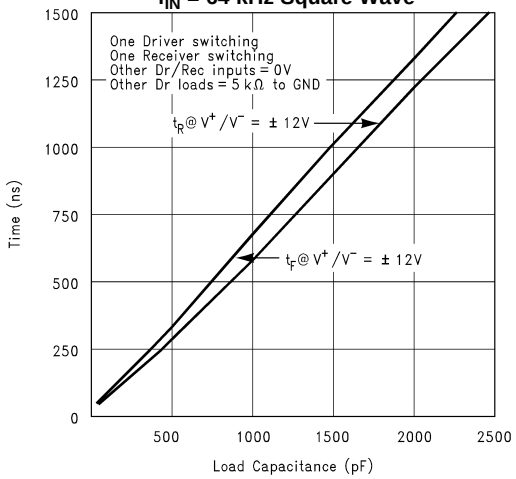


Figure 10.

Driver Output Voltage vs Frequency and C_L
Conditions: V_{CC} = 5V, R_L = 5 kΩ, T_A = 25°C

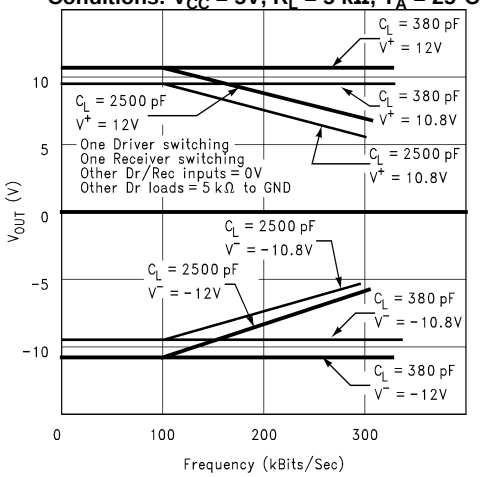


Figure 11.

Supply Current vs Frequency and Driver C_L

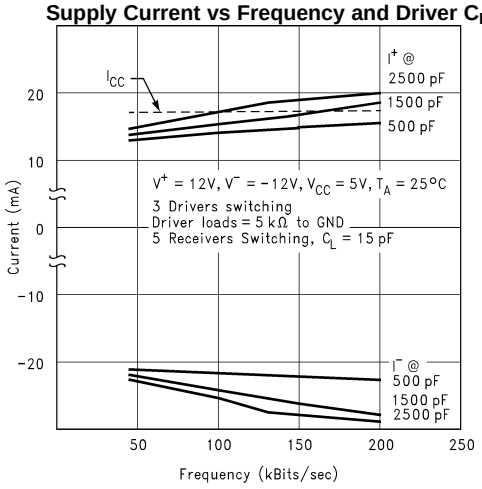


Figure 12.

Supply Current vs Frequency and Driver C_L

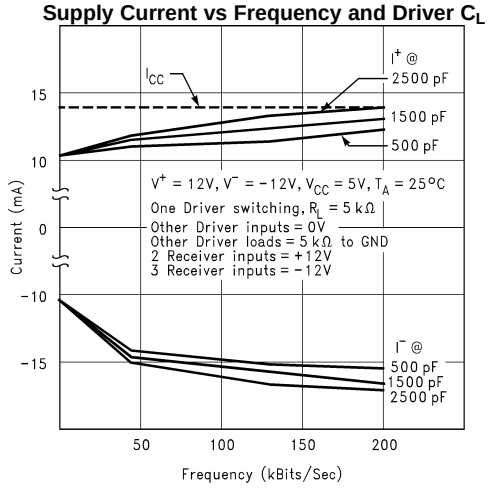


Figure 13.

Typical Performance Characteristics (continued)

Supply Current vs Frequency

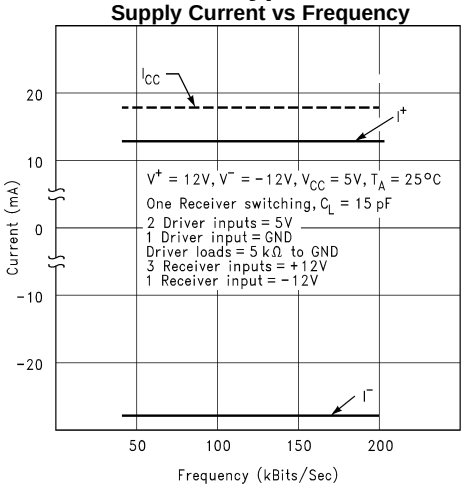


Figure 14.

Driver Output Current vs Output Voltage

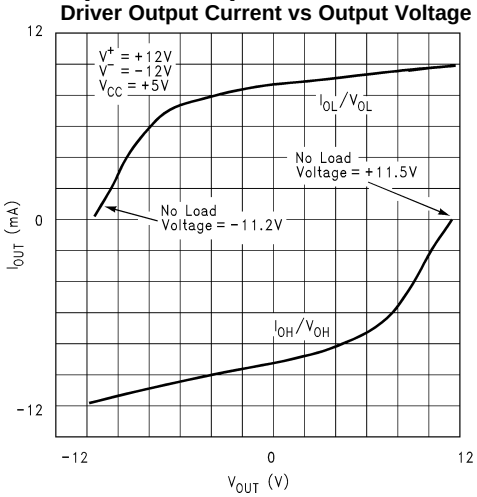


Figure 15.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS14185WM	LIFEBUY	SOIC	DW	20	36	TBD	Call TI	Call TI	0 to 70	DS14185WM	
DS14185WM/NOPB	LIFEBUY	SOIC	DW	20	36	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DS14185WM	
DS14185WMX/NOPB	LIFEBUY	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DS14185WM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

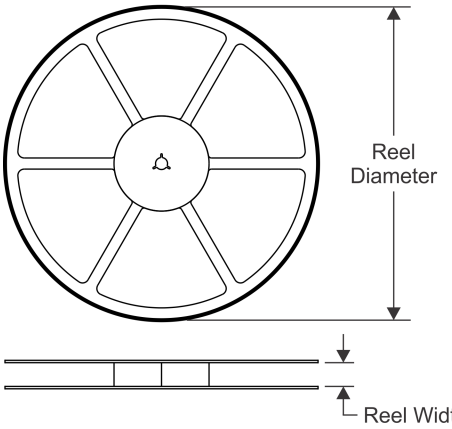
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

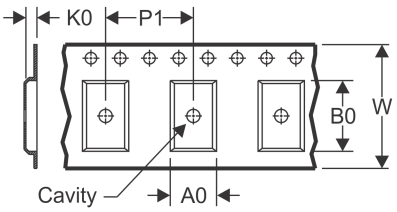
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

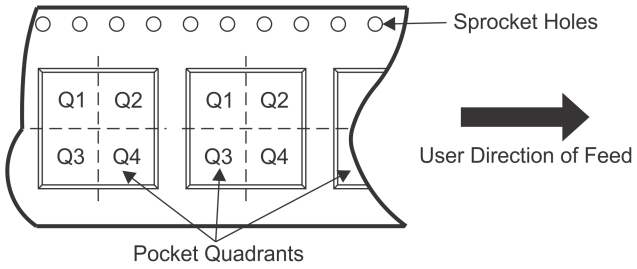


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

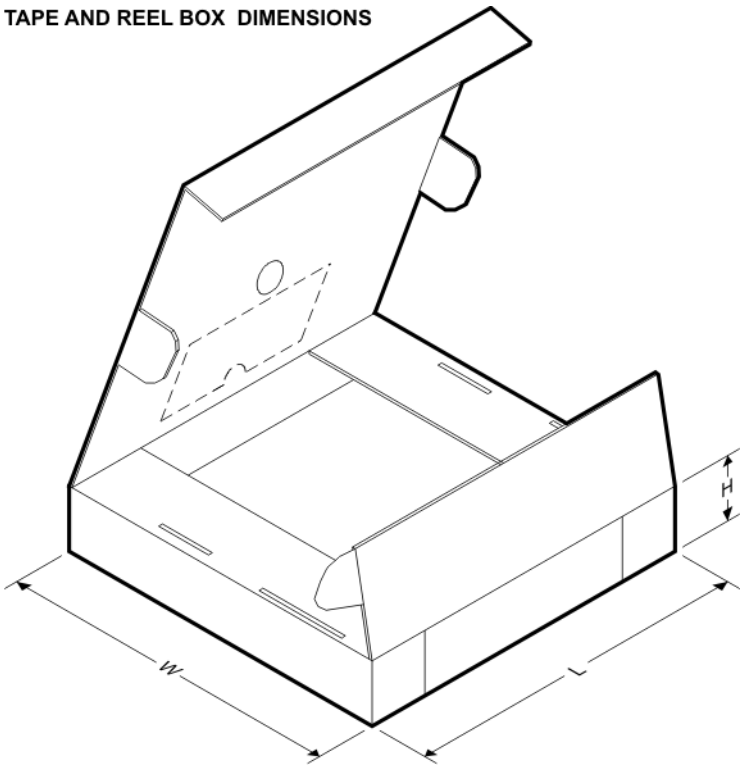
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

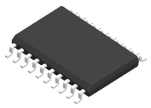
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS14185WMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS14185WMX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0

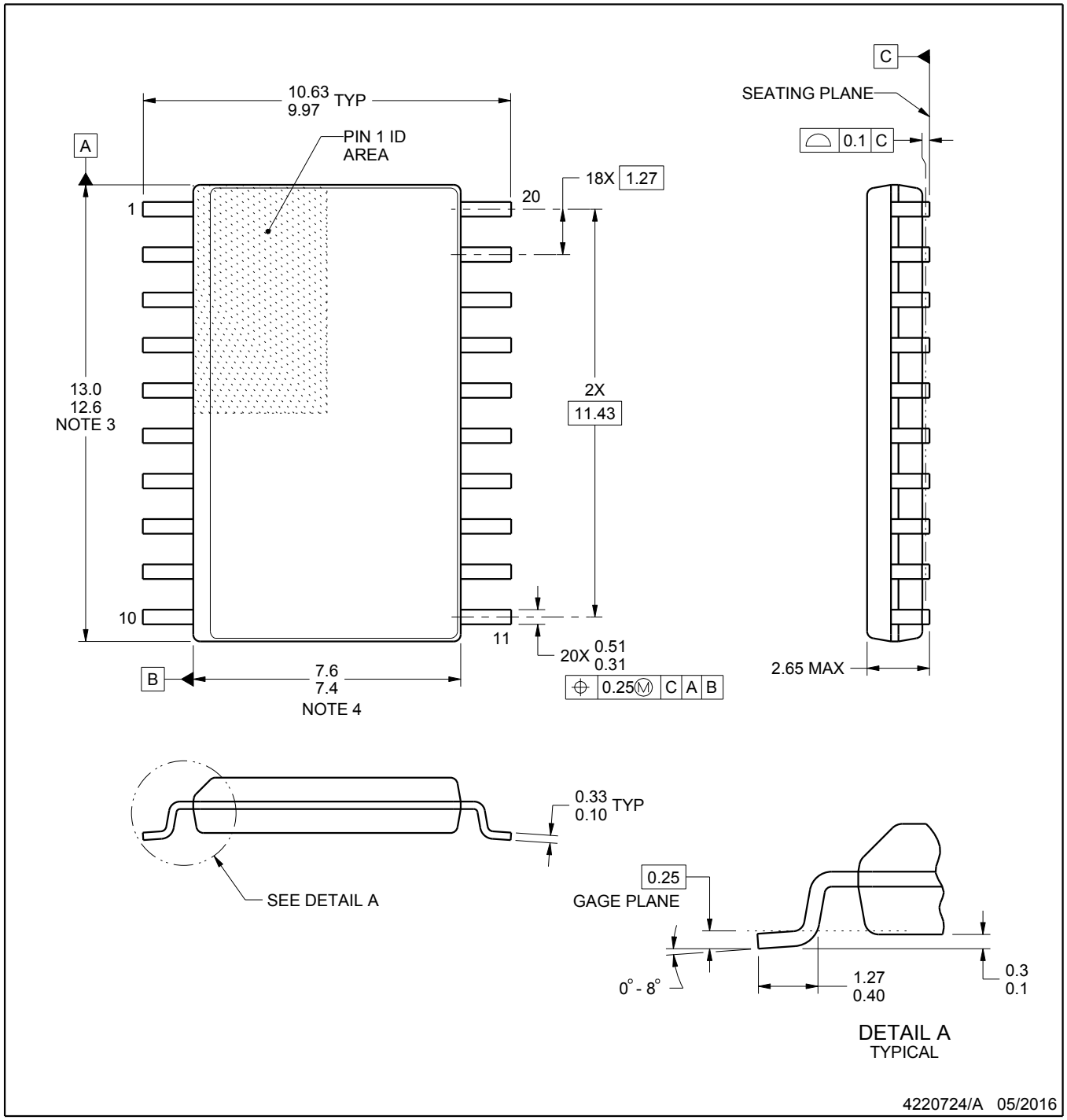


PACKAGE OUTLINE

DW0020A

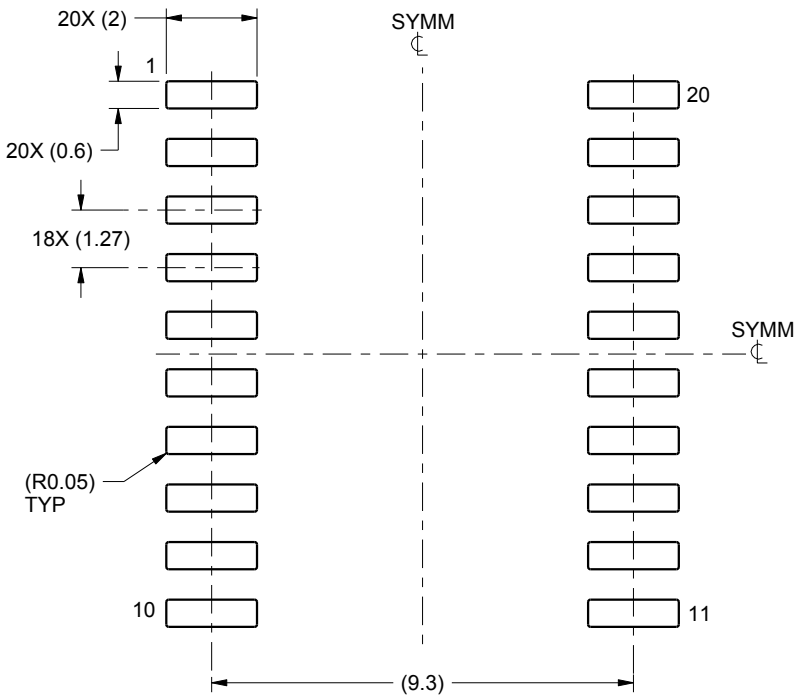
SOIC - 2.65 mm max height

SOIC

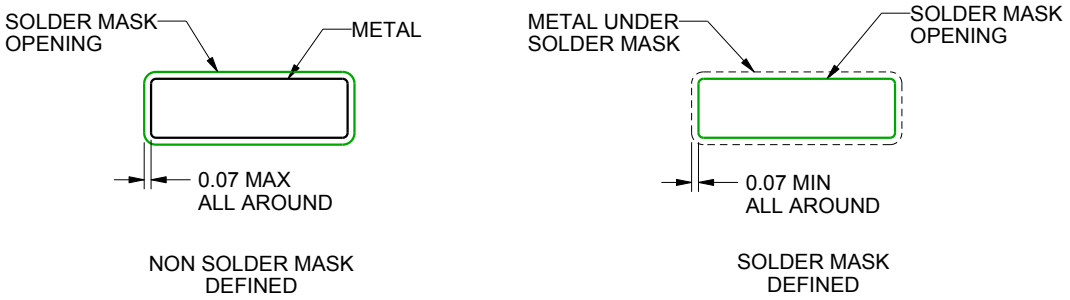


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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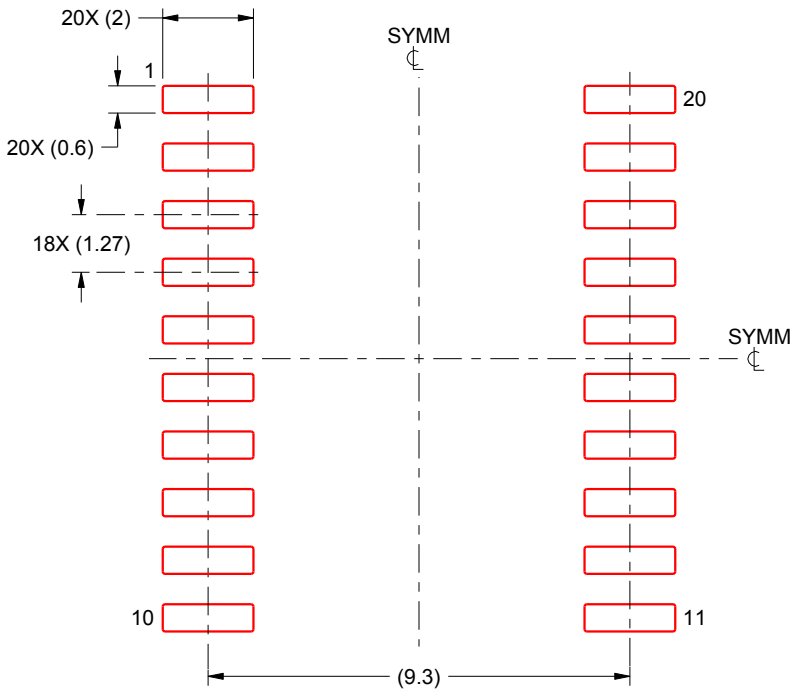
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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